International Journal of Innovative Technologies
WWW.IJITECH.ORG
ISSN 2321-8665
Vol.05,Issue.01,
January-2017,
Pages:0022-0027

Implementation of SFCC in HVDC Transmission System with Fault Tolerant Hybrid Converters

T. KARTHIK[1], G. SANJEEVA[2]
[1]PG Scholar, Vignana Bharathi Institute of Technology, Hyderabad, India, Email: karthikthota1992@gmail.com.
[2]Assistant Professor, Vignana Bharathi Institute of Technology, Hyderabad, India, Email: sanjeeva12.ies@gmail.com.

Abstract: With advancements in power engineering, load demand has also been increased form past few years. For higher load demand conditions AC transmission systems are not much recommended as there will be a increase in power loss during the transmission of high power. To overcome this issue HVDC transmission systems are introduced in the power engineering, stepping the voltage up to 765kV and transmitting larger powers to longer distances. With these high voltages of transmission, vulnerability to faults is also increased creating more damage to the equipment connected to the HVDC grid system. Since the recovery period for the dc link voltage is relatively long which causes severe damage to the grid system. In order to reduce the effect of faults in the grid system Hybrid power converters are introduced in series with the transmission lines with attachment of SFCC at the source ends. The SFCC has a current storage element (Inductor) which stores energy during fault conditions in the lines. The control of the SFCC depends on the amplitude of fault current in the transmission lines. The complete design and analysis is carried out in MATLAB Simulink software with all graphical representations and references.

Keywords: HVDC (High Voltage Direct Current), SFCC (Smart Fault Current Controller), MATLAB.

I. INTRODUCTION

Almost all HVDC transmission lines have been built as point-to-point interconnections. Many of them are designed to transfer large amount of power over long distances. A drawback of HVDC transmission systems is the difficulty of delivering energy at low cost to small and isolated ac loads that may be located in the vicinity of the HVDC power corridor [1]-[2]. The HVDC tap is an alternative solution to overcome the difficulty of delivering energy to relatively small, isolated ac loads. At the beginning, studies on tapping HVDC systems were carried out considering only inverters based on ordinary thyristors [1]–[3]. At that time, the series-tapped inverter arrangement was considered to be the more favorable solution since the shunt-tapped inverter can impact the operation of the main HVDC converter stations and was considered viable only for power ratings over 20% of the main stations. Later, particular attention has been given to gate turn-off thyristor (GTO)-based HVDC taps. Interesting results about parallel tap-off using GTO voltage source converters are reported in [4] and [5]. Here, a series dc–dc power converter is developed, employing soft-switching techniques.

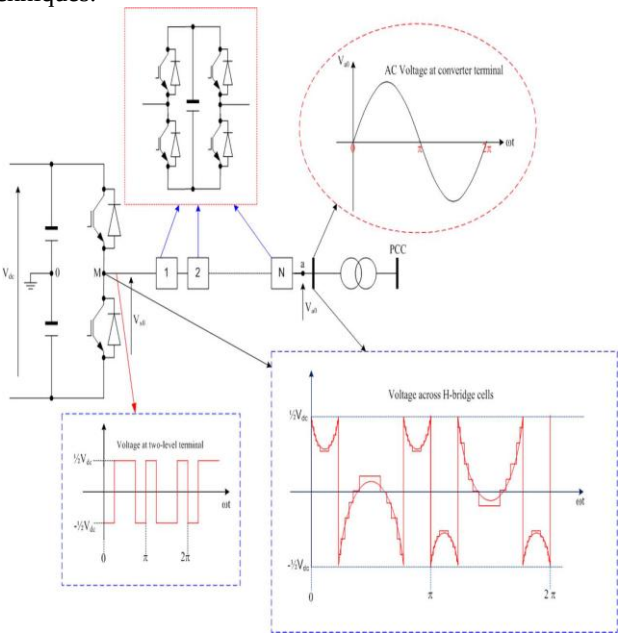

Fig. 1. HVDC system with hybrid converter.

Since the 1990s, a great deal of research effort has been directed to improving converters primarily to make them more power efficient than the first generation of voltage source converters(VSC) [5]–[8]. The modular multilevel converter (MMC), published in 1998 for STATCOM applications [9], published in 2003 for HVDC Power Transmission [10], and followed up in brought several new features to VSC. It replaced the series-connected insulated-gate biploar transistor (IGBT) in each arm of the two-level converter by a stack of half-bridge cells which consist of a charged capacitor and a set of IGBTs. Since the voltage of each cell is small compared to the ac and dc voltages, a large number of cells are placed in series in each stack, resulting in the creation of a voltage waveform with numerous steps. This characteristic has two main consequences: 1) the generated ac current is very close to a sine wave and no longer requires any filtering, thus saving the implementation of bulky and costly ac filters and 2) the converter does not rely on high-frequency

PWM to syntheses voltage waveforms, thus greatly reducing the switching loss and thereby improving the overall efficiency of the converter. Do not withstanding the advantages brought by this new generation of converters, there are some aspects that can still be improved.

The avoidance of the ac filter means that the cells are now one of the bulkiest components of the converter station and cell format requires a physically large capacitor in addition to the set of IGBTs. Half-bridge cells are normally used in preference to H-bridge cells (both illustrated in Fig. 1) in order to reduce the number of devices in conduction at any time and, therefore, reduce the conduction power loss. Even if this choice is justified by the large cost associated with the power losses, it also means that the converter is vulnerable to a dc-side fault in a similar way to a two-level converter whereas an H-bridge version would not be. The inability of half-bridge cells to produce a negative voltage results in the conduction of the antiparallel diodes connected to the IGBTs, thus creating an uncontrollable current path in case of a collapse of the dc bus voltage. Since the dc breakers for high-power applications are still under development the lack of other fast protective mechanisms makes this loss of a means to control dc fault current problematic. In the double-clamped submodule (DCS) was suggested as a new type of cell to deal with this issue. The DCS connects two half-bridge cells together into one cell through one additional IGBT and two diodes.

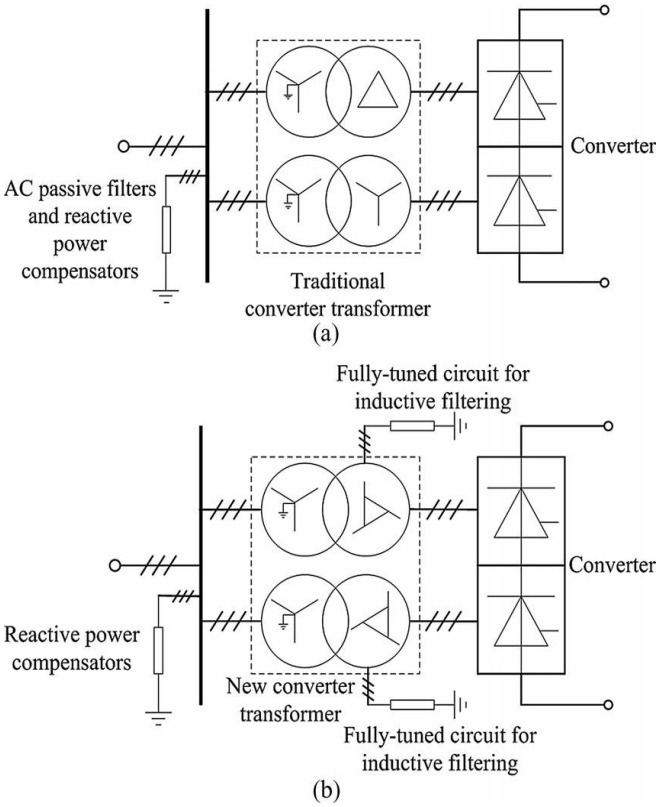

Fig. 2. Different HVDC systems.

This configuration offers the possibility of switching in a reverse voltage, similar to the H-bridge cell, in order to respond to the need for negative stack voltage in case of a dc-side fault. However the DCS does not fully solve the dc fault issue because: 1) only half the available positive voltage can be translated into negative voltage, leaving a voltage deficit from that needed to fully control the current and2) the power losses are increased by 50% compared to using two half-bridge cells during normal operation because of the additional IGBT in the conduction path. This paper presents the analysis of a new converter topology, which is part of a new generation of VSCs [4] based on the multilevel approach but also takes some characteristics from the two-level VSC. As explained through this paper, one of the features of this topology lies in its ability to retain control of the phase current during the loss of the dc-bus voltage, thanks to the presence of H-bridge cells in the arms as shown in Fig.2. The key advantage of this new topology lies in its reduced number of cells; thus, it does not compromise the efficiency of the converter, nor on the number of devices and even saves volume because of the reduced number of cells per arm. A component level simulation of a 20-MW converter is used to confirm the claimed characteristics of this new topology.

II. CONTROL OF HVDC SYSTEM

The intermediate control layer represents the current controller that regulates the active and reactive current components over the full operating range and restraints converter station current injection into ac network during network disturbances such as ac and dc side faults.

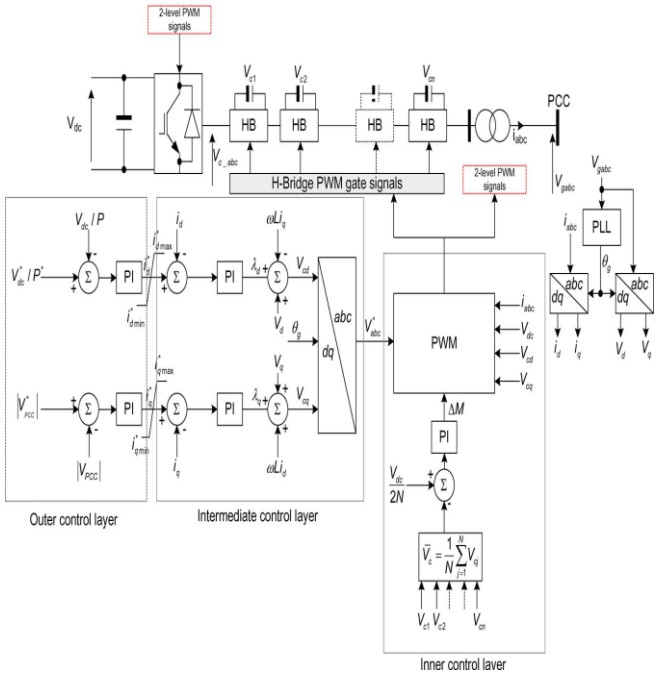

Fig. 3. Control structure of HVDC system.

The outer control layer is the dc voltage (or active power) and ac voltage (or reactive power) controller that provide set points [6] to the current controllers. The inner controller has only been discussed to a level appropriate to power systems engineers. The intermediate and outer control layers are presented in detail to give the reader a sense of HVDC control system complexity. The current, power, and dc link voltage controller gains are selected using root locus analysis, based

on the applicable transfer functions. Some of the controller gains obtained using root locus analysis give good performance in steady state but failed to provide acceptable network disturbance performance. Therefore, the simulation final gains [7] used are adjusted in the time domain to provide satisfactory performance over a wide operating range, including ac and dc side faults. Fig. 3 summarizes the control layers of the hybrid multilevel VSC.

III. SFCC CONFIGURATION

In General the abnormal current in the system (faults) are divided in to two types: first one is symmetrical and next classification is unsymmetrical fault (Line to Line fault, Line –Ground fault, Line-Line-Ground i.e. double line with ground fault). Because of breaking of the inductor or may due to the short circuit between these two inductors the abnormal current [3] in the electric system may occurs which tends to increase in current so power surges may occur. Basically Power surges is the problem of any power system which can lead to rapid overheating and loss of critical and expensive equipment. So due to abnormal current in the speed of the synchronous machine may decreases and system will go in to the dynamic again. If it is not possible to clear this fault in 1000 ms then it leads to Grid Failure. So it is very important to limit the fault below 1000ms so that here in this paper we propose the smart fault current controller (SFCC). The location of smart fault current controller is shown in the fig 4. The proposed fault current controller is made up of super conducting coil and four thyristors as shown in the fig 4. And a separate control unit is proposed in this SFCC.

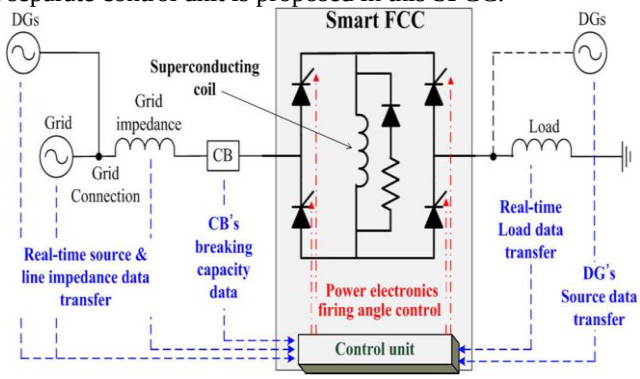

Fig. 4. SFCC configuration.

The smart FCC is based on solid-state and superconducting technology. It consists of a superconducting coil with a freewheeling diode if necessary, four thyristors, and a control unit. Fig. 4 shows the schematics deployed the smart FCC and a grid. Since the main topology is similar to a full-wave rectifier, called a bridge, the operational principle can be explained as a rectifier. The superconducting coil has no resistance and large inductance. Since the coil is a kind of energy storage, a current flowing the coil should be accumulated and then finally almost direct current (dc). It means there is no voltage drop across the coil in a normal operation. Note that the line current is ac and the coil current is dc. The dc coil current makes all thyristors turned on. Hence, the nominal ac current behave not to flow in the coil. In this case, the voltage drop is caused by just thyristors, or any other solid-state if replaced, since the coil is superconducting state and almost zero ac loss. On the other hand, when a fault occurs, the coil current should be increased. At this time, the large inductance of the coil reduces an abrupt surge at the first swing. After the first swing of half cycle, a control unit supplies controlled gate signals to the four thyristors. These gate signal delay can adjust the fault current level. In a range of 0 to 180 degrees, the delay angle can be selected. For example, if the delay is 0 degree, this FCC operates like a bridge-type SFCL employing power diodes, so-called a dc reactor type SFCL. If the delay is 180 degrees, there is no signal to any thyristors, which means line current is cut off. Fig. 5 shows one example of fault controlling based on a simulation. These two charts are both in a case of 90 degrees delay. As shown in the graphs, after the first peak, the line current was controlled by the firing angle delay.

The most important part of the smart FCC system is the control unit. All information about the grid network related to the smart FCC can be transferred to the control unit as Fig. 4. The information can be converted to an equivalent value such as Thevenin impedance and load current in the line. The control unit can calculate the optimal fault current level based on the collected data. The existing protection devices, such as over current relays and circuit breakers, should be considered when the calculation of the optimum fault level is performed. Since the generating source capacity has a temporal variation when DGs are connected to the grid, the optimum delay angle should be calculated every collection of the information. That is, real-time optimal firing angle is being calculated and ready to supply to the gate signals. When a fault occurs, the coil current should be increased. Then, the controller can recognize an event of the fault. The gate signals can be controlled based on the updated optimal firing angle delay. The firing angle can be modified even during the fault in order to satisfy with the optimal fault current level by considering the interrupting duty of breakers and time delay before interruption.

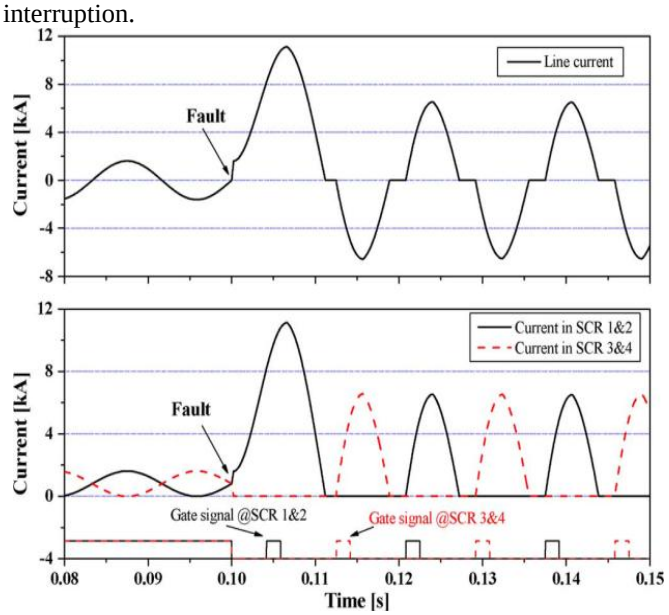

Fig. 5. Current suppression with SFCC.

IV. SIMULINK RESULTS AND OUTPUTS

Simulation results of this paper is as shown in bellow Figs.6 to 10.

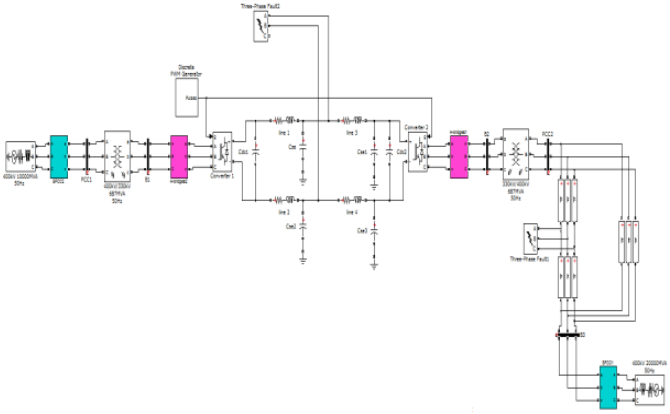

Fig. 6. HVDC test system with Hybrid converters.

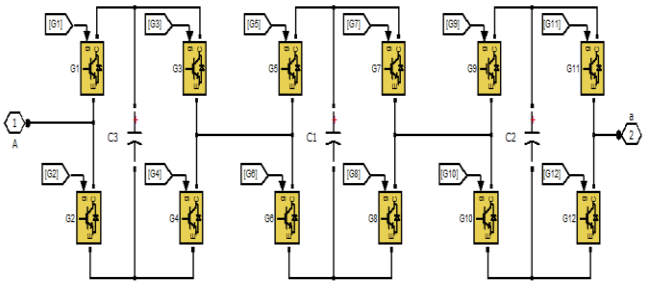

Fig. 7.Three module hybrid converters.

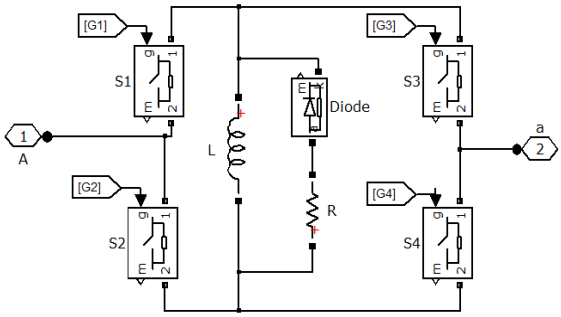

Fig. 8. SFCC model of Simulink.

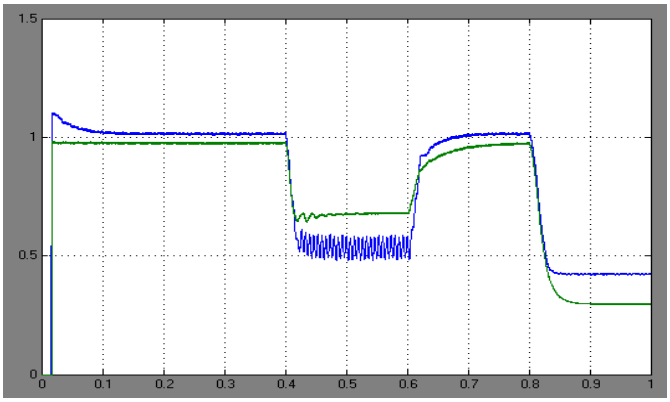

Fig. 9. Network 2 voltage magnitude comparison without and with SFCC during fault.

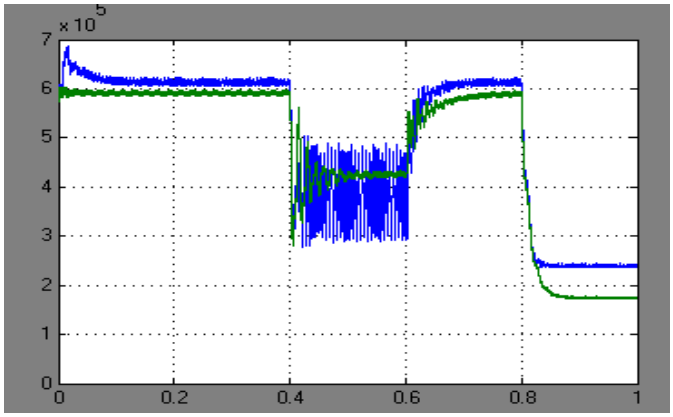

Fig. 10. DC voltage with and without SFCC during fault.

V. CONCLUSION

With the above results of the HVDC test system with fault at AC line and DC line the comparison of AC voltage and DC voltage is taken. It can be clearly observed that the voltage drop is reduced with SFCC during AC fault (0.4-0.6sec) and also during DC fault (0.8-1sec) on both AC and HVDC transmission line.

VI. REFERENCES

[1]G.P.Adametal.,"Network fault tolerant voltage-source-convertersforhigh-voltageapplications,"inProc.9thIETInt. Conf. ACandDCPowerTransmission,London,U.K.,2010,pp.1–5.

[2]Y.Zhangetal.,"Voltagesourceconverterinhighvoltageapplications:Multilevelversustwo-levelconverters,"inProc. 9th IETInt. Conf.ACandDCPowerTransmission,London,U.K.,2010,pp.1–5.

[3]G.P.Adametal.,"Modularmultilevelinverter:Pulsewidthmodulationandcapacitorbalancingtechnique,"IETPowerElectron.,vol.3,pp.702–715,2010.

[4]M.M.C.Merlinetal.,"Anewhybridmulti-levelvoltage-source converterwithDCfaultblockingcapability,"inProc.9thIETInt.Conf.ACandDCPowerTransmission,London,U.K.,2010,pp.1–5.

[5]G.P.Adametal.,"Modularmultilevelconverterformedium-voltageapplications,"inProc.IEEEInt.Conf.Electr.Mach.Drives Conf.,2011,pp.1013–1018.

[6]G.P.Adam,S.J.Finney,A.M.Massoud,andB.W.Williams,"Capacitorbalanceissuesofthediode-clamped multilevel inverter operated in aquasi-two-statemode, "IEEETrans. Ind. Electron., vol.55,no.8,pp.3088–3099,Aug.2008.

[7]M.Chavesetal.,"Newapproachinback-to-backm-level diode clamped multilevel converter modelling and direct current busvoltagesbalancing,"IETPowerElectron.,vol.3,pp.578–589,2010.

[8]S.R.Lee,J.Kim,J.Yoon,andB.Lee,"Conceptdesignofsuperconductingpowersystemapplyingdistributedswitchingstationsforthemetropolitanarea,"IEEETrans.Appl.Supercond.,vol.19,no.3,pp.2057–2061,Jun.2009.

[9]J.A.Waynert,H.J.Boenig,C.H.Mielke,J.O.Willis,andB.L.Burley,"RestorationandtestingofanHTSfaultcurrentcontroller,"IEEETrans.Appl.Supercond.,vol.13,no.2,pp.1984–1987, Jun. 2003.

[10]S.A.Papathanassiou,"Atechnicalevaluationframeworkfort heconnectionofDGtothedistributionnetwork,"ElectricPowerSy stemsResearch,vol.77,pp.24–34,2007.
[11]TheSmartGrid:AnIntroduction,LitosStrategicCommunicat ionforUSDepartmentofEnergyp.11,2008.

Author's Profile:

T. Karthik was graduated in 2014 in first class with distiction from Ganapathy college of engineering affiliated to JNTU-HYD in Electrical and Electronics Engineering. He is pursuing his post graduate degree in power systems from JNTU-HYD. His research interest is FACTs devices, Harmonic compensation technology, multi bus sytems, fault tolerance on power systems.

G Sanjeeva was graduated in 2011 in first class from Nalla Malla Reddy Engineering College affiliated to JNTU-HYD in Electrical and Electronics Engineering. He took his post graduate degree in 2014 from JNTU-HYD in power systems. His research interest is Load frequency control, Distribution systems and Renewable energy resources.