# *AN ON- CHIP DELAY MEASUREMENT TECHNIQUE USING SIGNATURE REGISTERS FOR SMALL- DELAY DEFECT DETECTION*

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**ABSTRACT**- *This paper presents a delay measurement technique using signature analysis, and a scan design for the proposed delay measurement technique to detect small-delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors. The evaluation with Rohm 0.18- m process shows that the measurement time is 67.8% reduced compared with that of the delay measurement with standard scan design on average. The area overhead is 23.4% larger than that of the delay measurement architecture using standard scan design, and the difference of the area overhead between enhanced scan design and the proposed method is 7.4% on average. The data volume is 2.2 times of that of test set for normal testing on average.*

***Index Terms****—Delay estimation, design for testability (DFT), integrated circuit measurements, semiconductor device reliability, Signature register*

## 1. INTRODUCTION

This paper presents a delay measurement technique using signature analysis, and a scan design for the proposed delay measurement technique to detect small-delay defects. The pro- posed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors. The evaluation with Rohm 0.18-μm process shows that the measurement time is 67.8% reduced compared with that of the delay measurement with standard scan design on average. The area overhead is 23.4% larger than that of the delay measurement architecture using standard scan design, and the difference of the area overhead between enhanced scan design and the proposed method is 7.4% on average. The data volume is 2.2 times of that of test set for normal testing on average.

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems [1]. If small-delay defects cannot be detected in LSI screening, the chips will behave abnormally under particular operations in certain applications, and their lifetime may become very short due to the vulnerability to the transistor aging. Therefore to keep the reliability after shipping, enhancing the quality of the testing for the small-delay defect detection is an urgent need. The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects [2]. However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. Therefore development of the embedded delay measurement technique is required.

Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques [3]. In this technique, the delay of a path is measured by continuous

sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flipflop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation. However, it has a drawback. The measurement time of the technique depends on the time for the scan operation. These days, the gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical. Noguchi et al.proposed the self testing scan-FF. The flip flop reduces the required number of scan operations, which makes the measurement time practical [2]. They also proposed the area reduction technique of the self testing scan-FF [4]. However, the area overhead of these methods is still expensive compared with the conventional scan designs.

## 2 ARCHITECTURE

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems. If small-delay defects cannot be detected in LSI screening, the chips will behave abnormally under particular operations in certain applications, and their lifetime may become very short due to the vulnerability to the transistor aging. Therefore to keep the reliability after shipping, enhancing the quality of the testing for the small-delay defect detection is an urgent need. The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects. However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. Therefore development of the embedded delay measurement technique is required. Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques.

### 2.1 Variable clock generator

In the proposed method, the clock width should be reduced continuously by a constant interval as explained later. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator is indispensable for the proposed method. In this paper, we use the on-chip variable clock generator proposed by Noguchi *et al* .Fig. 1 illustrates the circuit. The circuit consists of the phase interpolator-based clock generator and the 2-pulse generator. The phase-interpolator-based clock generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal.

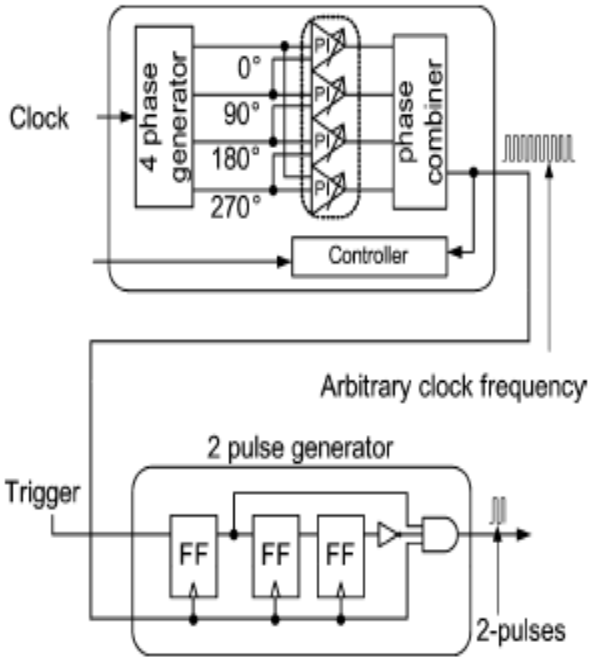


**Fig.2.1: Circuits with Phase interpolator-based clock**

# 3 PROPOSED METHOD

## 3.1 small-Delays Defect Detection with Delay Measurement of Chips

The proposed method uses the Noguchi's small-delay defect detection technique. In this technique, the test clock width for delay fault testing of each path is determined with the normal path-delay distribution of each path. This strategy has already been applied to various small-delay detection techniques. But its originality is to obtain the path-delay distribution with the delay measurement of the paths of the fabricated chips. Fig. 2.2 shows the path delay distribution of a path obtained by the delay measurement of the fabricated sample chips. The horizontal axis is measured delay. The vertical axis is the number of chips. The chips which have delay inside the range Variation are normal chips. The chips which have delay outside the range Variation, namely, are abnormal chips. The delay is the outside of the clock cycle in normal operation. Therefore it will be detected by conventional delay fault testing with the clock cycle in normal clock operation which is Conventional criteria.

The delay and are within the clock cycle in normal operation. In Noguchi's technique, the test clock cycle is set to the upper limit of the distribution of normal chips, which is a new criterion. Then all the outlier chips are detected by the delay fault testing. In small technology, the path-delay distribution calculated by simulation is different from that of the fabricated chips. Therefore the quality of its strategy is higher than that of simulation based ones. Because the Noguchi's technique requires the measurement of the explicit paths, the paths should be single-path sensitizable. The aim of the technique is to screen the chips which have abnormal delay in gates or wires. Therefore the test set for the measurement should detect all the transition faults which are sensitized through single-path sensitizable paths. The proposed method is a new delay measurement technique for the small-delay defect detection technique.

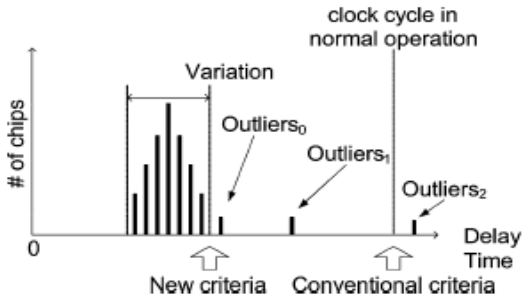


**Fig. 3.1: Decision of test clock width based on path delay distribution obtained by chip measurement**

## 3.2 Delay Measurement Technique Using Signature Registers

This section explains the proposed measurement method. Section III-A presents the concepts of the proposed method. Section III-B explains the implementation of the proposed method. Section III-C describes the measurement sequence. The data volume and area overhead should be realistic compared with the conventional scan designs for DFT. Section III-D explains the reduction method of the tester channel. Section III-E describes the scheme for the decision of the number of the required extra latches to keep the cost realistic. To apply the proposed method and realize short measurement time, some constraints should be put on ATPG. Section III-F explains the ATPG constraints. Section III-G describes the measurement time and data volume. Finally, Section III-H describes the test response tracing mode for finding lowest failing frequency or diagnosis with transition fault test vectors.

### *Basics*

This section explains the concept of the proposed delay measurement. The target paths of the proposed method are single path sensitizable. Basically, the proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement.

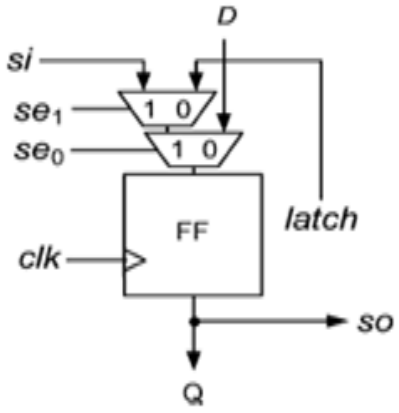


**Fig: 3.2 Scan Flip Flops For Proposed Measurement**

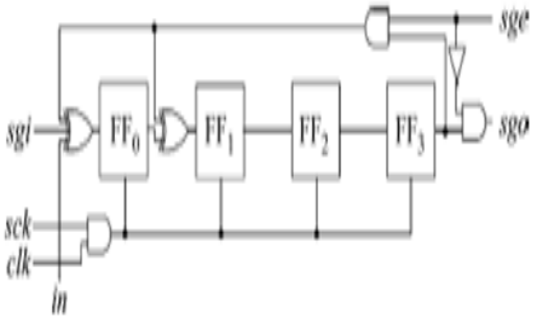


**Fig :3.3 Four bit Reconfigurable signature register**

Here, we measure the delay of. In this example, we assume that the clock width of normal operation is 10 ns, and the resolution of the delay measurement is 2 ns. First, SIG is initialized with reset operation. Second, the target path is tested continuously 5 times with the test clock reduced gradually by the resolution. The multiple clock width testing is realized by the variable clock generator explained in Section II-B. The test clock of the 1st testing (#1) is 10 ns. After the test, the test response is sent to SIG through the scan path with two clock shift out operation. The test clock of the second testing (#2) is 8 ns. Similarly, the test clock width of the third, fourth, and fifth testings (#3, #4, #5) are the difference between 2 ns and the previous test clock width. Each test response is sent to SIG with two clocks. After the above 5 times of delay fault testing's, the signature value of SIG is retrieved.

## 4. SIMULATION RESULTS

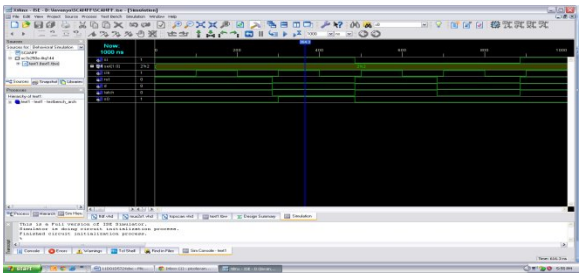

**Fig: 4.1 Simulation results of proposed scan flipflop**

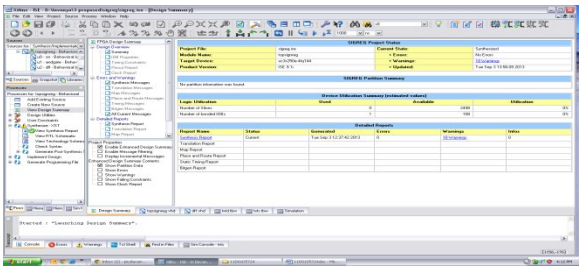

**Fig 4.2 design summary of proposed scan flipflop**

## 5. CONCLUSION

The proposals of this paper are as follows. The proposal of the delay measurement method using signature analysis and variable clock generator. The proposal of a scan design for the delay measurement of internal paths of SoC. The first proposal can be applied not only SOC but also field programmable gate array (FPGA). Because the process of FPGA is getting extraordinary smaller these days, the small delay defect becomes serious problem in FPGA, too. In this meaning, the application of the proposed method to FPGA is also useful. A future work is the low cost application of the proposed measurement to FPGA. When we measure short paths the measurement error can increase for the IR drop induced by higher test clock frequency. It can reduce the test quality. Another future work is the reduction and the avoidance of the measurement error caused by the IR drop.

## 6. REFERENCES

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