A High Frequency Cascaded Multilevel Inverter with ZVS Active Clamped Isolated DC-DC Converter

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Abstract: Utilization of high frequency in AC transmission of power reveals more advantages than the medium and lower frequency AC transmission. In renewable application and storage devices several inverters are used where PWM in employed. The usage of these inverter increases the THD in the grid, to overcome these problems in this paper we introduce a novel converter multilevel inverter generates high frequency multilevel AC output voltage. The input is fed with a ZVS active clamped isolated DC-DC converter to decrease the DC voltage regulation. The total design and analysis is carried out in MATLAB Simulink software with all graphical representation in results.

Keywords: Zero-Voltage Switching (ZVS), High-Frequency (HF), Switched-Capacitor (SC).

I. INTRODUCTION

Even though renewable energy sources like solar and wind energy are available free of cost, their output is not secure due to their intermittent nature. Fuel cells output is secure and continuous in all seasons as long as the continuity of fuel supply is maintained and produce heat as byproduct that can be used for co-generation/heating and thus increases the overall efficiency of the system. Distributed generation for standalone and grid-tied applications for residential and remote power systems are important applications. Two-stage inverter, i.e. high-frequency (HF) transformer isolated dc/dc converter followed by an inverter has been adopted by industries and has been proposed with different configurations and modulations in literature to achieve the given objectives. HF transformer isolated dc/dc converter translates the low fuel cell stack voltage to higher than the peak of the utility line or inverter output voltage specification with necessary isolation. Soft-switching is necessary to operate the converter at HF and to realize small size, light weight and low cost converter. It reduces the thermal stress on the components, switching losses, and improves the efficiency, particularly at light load where the switching and conduction losses are comparable or switching losses dominate the conduction losses. Many dc/dc converter topologies have been presented for this application but most of them are not able to maintain soft-switching over the wide power variation and entire operating range of fuel-cell voltage.

Converter presented is hard-switched and two devices are connected in parallel to improve the efficiency and switching frequency is 50 kHz. Interleaved current-fed full-bridge converter reported is a hard-switched converter and therefore operated at 10 kHz, which increases the size of magnetics/filters and therefore, of the converter. Full-bridge voltage-fed converter has several problems: rectifier diode ringing, duty cycle loss, snubber across secondary, pulsating current at input increases filter size and has limited zero-voltage switching (ZVS) range. Many additional components are used to achieve ZVS which is not a simpler solution and exhibits lower efficiency. A topology similar to is presented, but secondary side switches lose ZVS at light load and higher input voltage, the ZVS range is calculated. A non-isolated bidirectional converter with active-clamping has been proposed for ZVS up to 40% load but operation with wide input voltage variation is not reported. A solution to achieve ZVS over 1:2 source voltage variation using several extra components is given without discussing ZVS for variation in load. A comparison of soft-switched dc/dc converters for fuel cells to utility interface is given and it was shown that a two-inductor half-bridge current-fed isolated dc/dc converter with active-clamp is suitable for such applications.

Active-clamp snubs the voltage turn-off spike and aids in ZVS of HF switches but cannot maintain ZVS for the wide operating range of load and input voltage. Also, it has power limitation and is not modular. Full-bridge current-fed topology is modular in nature and is easy to be interleaved due to single inductor topology with less sensor requirements and less state variable and is suitable for high power. It should be noted that the magnetizing inductance makes the transformer leakage inductance current continuous and also increases the number of state variables. Therefore, the operation, analysis and design get modified due to the third state variable and this was completely neglected in the earlier analysis and design. However, the analysis and design for full range ZVS is not mentioned. To achieve ZVS for wide variation in input voltage and load while maintaining high efficiency has been a challenge, especially for low voltage higher current input applications. This paper introduces a design as a solution to cover ZVS for wide operating range.
Hard-switching topology for low switching frequency operation is discussed as shown in Fig. 1.

![Fig. 1. ZVS active clamped DC-DC converter.](Image)

II. NOVEL CASCADED MULTI LEVEL INVERTER

The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor-clamped type. The former uses diodes to clamp the voltage level, and the latter uses additional capacitors to clamp the voltage. The higher number of voltage levels can then be obtained; however, the circuit becomes extremely complex in these two topologies. Another kind of multilevel inverter is cascaded H-Bridge constructed by the series connection of H-Bridges. The basic circuit is similar to the classical H-bridge DC-DC converter. The cascaded structure increases the system reliability because of the same circuit cell, control structure and modulation. However, the disadvantages confronted by cascaded structure are more switches and a number of inputs as shown in Fig. 2. In order to increase two voltage levels in staircase output, an H-Bridge constructed by four power switches and an individual input are needed. Theoretically, cascaded H-Bridge can obtain staircase output with any number of voltage levels, but it is inappropriate to the applications of cost saving and input limitation. A number of studies have been performed to increase the number of voltage levels. A switched-capacitor (SC) based multilevel circuit can effectively increase the number of voltage levels. However, the control strategy is complex, and EMI issue becomes worse due to the discontinuous input current.

A single-phase five level pulse width-modulated (PWM) inverter is constituted by a full bridge of diodes, two capacitors and a switch. However, it only provides output with five voltage levels, and higher number of voltage levels is limited by circuit structure. An SC-based cascaded inverter was presented with SC front-end and full bridge backend. However, both complicated control and increased components limit its application. The further study was presented using series/parallel conversion of SC. However, it is inappropriate to the applications with HF output because of multicarrier PWM (MPWM). If output frequency is around 20 kHz, the carrier frequency reaches a couple of megahertz. Namely, the carrier frequency in MPWM is dozens times of the output frequency. Since the carrier frequency determines the switching frequency, a high switching loss is inevitable for the sake of high-frequency output. A boost multilevel inverter based in partial charging of SC can increase the number of voltage levels theoretically. However, the control strategy is complicated to implement partial charging. Therefore, it is a challenging task to present an SC-based multilevel inverter with high-frequency output, low-output harmonics, and high conversion efficiency.

Based on the study situation aforementioned, a novel multilevel inverter and simple modulation strategy are presented to serve as HF power source. The rest of this paper is organized as follows. The discussions of nine-level inverter are presented in Section II, including circuit topology, modulation strategy, operation cycle, and Fourier analysis. The parameter determination and loss analysis are discussed in Section III.

![Fig. 2. Novel cascaded multilevel inverter with HFAC output.](Image)

III. OPERATING MODES OF INVERTER

Fig. 3 demonstrates the ideal waveforms of proposed inverter. \( V_c \) is the triangular carrier, and \( V_{in} \) is the peak value of \( V_c \). The modulation signals of triangular carrier are \( V_m, 1c, V_m, 1b, V_m, 2c \) and \( V_m, 2b \). \( V_m, 1b \) and \( V_m, 2b \) are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and \( \delta \) is the duration of voltage levels controlled by them. \( V_m, 1c \) and \( V_m, 2c \) are used to control the alternative operations of \( S_1 \) and \( S_2 \), respectively, and \( \theta \) is the duration of voltage levels controlled by them. Thus, the drive signals of H-Bridge switches (\( S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, S_{2d} \)) are phase-shifted pulse signals, while the drive signals of SC switches (\( S_1, S_2, S_3, S_4 \)) are complementary pulse signals. Two operational modes are presented as shown in Fig. 3(a) and (b). Mode 1 is similar to mode 2 apart from the different positions of modulation signals (\( V_m, 1c, V_m, 1b, V_m, 2c, V_m, 2b \)). Consequently, the durations of each voltage level are controlled by modulation signals in both mode 1 and mode 2. Active circuits of the operational mode 1 are demonstrated in Fig. 4. Re is the equivalent load. When \( t \) satisfies \( t_0 \leq t < t_1 \) in Fig. 3, the switches \( S_{1a}, S_{1b}, S_{2a}, S_{2b} \) are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in freewheeling state, and output voltage equals 0. Because \( S_1 \) and \( S_2 \) are on, the capacitors \( C_1 \) and \( C_2 \) are charged to \( V_{in} \) (\( V_{dc1} = V_{dc2} = V_{in} \)). The voltages on Bus 1 and Bus 2 are \( V_{in} \) as well. The current flow of this time interval is shown in Fig. 4(a). When \( t \) satisfies \( t_1 \leq t < t_2 \) in Fig. 3, the switches \( S_{1a}, S_{1b}, S_{2a}, S_{2c} \) are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive conducting state. Output voltage equals \( V_{in} \). Because \( S_1 \) and \( S_2 \) are on, the capacitors \( C_1 \) and \( C_2 \) keep charged to \( V_{in} \) (\( V_{dc1} = V_{dc2} = V_{in} \)). The voltages on Bus 1
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When \( t \) satisfies \( t_2 \leq t < t_3 \) in Fig. 3, the switches \( S_{1a}, S_{1c}, S_{2a}, S_{2c} \) are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state.

Output voltage equals \( 2V_{\text{in}} \). Because \( S_1 \) and \( S_2 \) are on, the capacitors \( C_1 \) and \( C_2 \) keep charged to \( V_{\text{in}} \left( V_{dc1} = V_{dc2} = V_{\text{in}} \right) \). The voltages on Bus 1 and Bus 2 are \( V_{\text{in}} \) as well. The current flow of this time interval is shown in Fig. 4(b).

The second half-cycle (from \( t_8 \) on) has the similar active circuits as the first half-cycle (\( t_1 - t_8 \)), but the current will be circulated in the opposite direction to provide the negative output voltage. The relations of on-state switches and output voltage level are described in Table I, as well as operations of two modes are compared closely. Table I have ten working states for nine voltage levels. When the operation enters a new state from an adjacent state, only one power switch changes between on and off. The device stress in switching devices of H-bridge circuit is higher than that in SC circuit. It can also be found that the output voltage in Mode 1 is more stable than Mode 2 due to less discharging period of switching capacitor. Along with the up-down movement of modulation signals (\( V_{m1c}, V_{m1b}, V_{m2c}, V_{m2b} \)), the output voltage of the proposed inverter is a controllable nine-level staircase. The duration of each voltage level is determined by the duty-cycle of SC circuit and the phase-shifted angle of H-Bridge circuit.
IV. SIMULINK RESULTS

Fig. 5. Novel cascaded HFAC inverter with ZVS active clamped DC-DC converter.

The above Fig.5 is the Simulink model of high frequency cascaded multilevel inverter with ZVS active clamped isolated DC-DC converter which is designed in the matlab.

Fig. 6. ZVS active clamped DC-DC converter DC output voltage.

Fig.6 shows the output voltage of the ZVS active clamped DC-DC converter which is a DC output voltage. Fig. 7 shows the Control of cascaded HFAC inverter.

Fig.7. Control of cascaded HFAC inverter.

Fig. 8. Switching pattern generation of cascaded multilevel inverter.

Fig.8 shows the switching pulses of cascaded multilevel inverter and the output voltage of the cascaded multilevel inverter.

Fig. 9. Boosted cascaded multilevel inverter HFAC output.

Fig.9 shows the output voltage of the cascaded multilevel inverter of ZVS active clamped isolated dc-dc converter. Fig. 10 shows the THD analysis of multilevel output voltage.
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Fig. 10. THD analysis of multilevel output voltage.

V. CONCLUSION

The ZVS active clamped DC-DC converter thus increased the DC output voltage with a high gain of ‘9’ times that of the input voltage with very less ripple. The high gain DC voltage output of the ZVS converter is further fed to the HFAC inverter with nine level output with a frequency of 25 kHz. The THD of the HFAC cascaded multilevel inverter is calculated to be 21.23% analyzed through FFT analysis in power GUI tool. Thus with a high gain and high frequency output of the novel topology, can be implemented in many renewable and storage DC sources.

VI. REFERENCES