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Architecture for Testability of Sleep Convention Logic

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Abstract: Testability is a noteworthy worry in industry for the present complex framework on-chip outline. Plan for-testability (DFT) procedures are basic for any rationale style, incorporating offbeat rationale styles so as to lessen the test cost. Rest tradition rationale (SCL) is another promising offbeat rationale style that depends on the all the more outstanding nonconcurrent rationale style NULL tradition rationale (NCL). As opposed to the NCL, there are right now no plan for testability approachs existing for the SCL. The point of this paper is to break down the different flaws within SCL pipelinesand proposea check based DFTmethodology to make the SCLtestable. Theproposed DFT technique is then approved through various investigations, demonstrating that the philosophy gives a high test scope (>99%). The total DFT philosophy and additionally the output chain and sweep cell configuration are exhibited.

Keywords: Design For Testability (DFT), Multithreshold NULL Tradition Rationale (MTNCL), NULL Tradition Rationale (NCL), Rest Tradition Rationale (SCL).

I. INTRODUCTION

SLEEP convention logic (SCL), also known as multi-threshold NULL convention logic (MTNCL) [1]–[4], is a variant of NULL convention logic (NCL) [5], [6] that takes advantage of the Multi-Threshold Complementary Metal Oxide Semiconductor (MTCMOS) power-gating technique [7][8] to further reduce the power consumption. The application of MTCMOS to the NCL circuits comes with interesting architectural changes that ultimately results in area and performance advantages as well. Similar to most other asynchronous logic styles, SCL is not supported by the current synchronous Automatic Test Pattern Generation (ATPG) tools [9]. This is due to a number of major changes in the circuit architecture, such as using asynchronous handshaking signals instead of a global clock for synchronization, using multirail encoding to represent signals, and using threshold gates instead of traditional Boolean gates. Design for testability (DFT) is a major concern in today's semiconductor industry because it is essential to reduce test time, increase test quality, and reduce the cost associated with generating and applying test vectors. In contrast to the NCL circuits, no DFT methodology has been developed for the SCL circuits so far. The current NCL specific DFT techniques cannot be directly used for the SCL circuits due to the structural differences caused by introducing the sleep mechanism for power-gating. The aim of this paper is to analyze the various stuck-at faults within an SCL pipeline and propose comprehensive scan-based testing methodology that provides for a high test coverage at the cost of the usual area overheard caused by introducing the scan chain.

II. LITERATURE SURVEY

Current ATPG tools do not support asynchronous circuit styles such as the NCL due to asynchronous feedback paths and absence of a clock signal. There are mainly two approaches in the literature to make the NCL circuits testable: limited insertion of control/observation points to increase fault coverage [3], [4], and synchronous modeling of NCL pipelines to make them compatible with synchronous ATPG tools and using scan chain technique [5]. Limited Insertion of Control/Observation Points: The first approach to make the NCL circuits testable focuses on finding nodes that are not easily controllable or observable and then inserts additional control signals or observation points to improve testability. For example, the output of each completion detector in the NCL pipeline is connected to the register of the previous stage. This creates an asynchronous feedback path that is not easily controllable by synchronous ATPG tools especially when the signal is buried in a deep pipeline. Breaking the feedback path and inserting an XOR gate controlled by a primary input provides a test point that improves controllability. Moreover, in the NCL pipeline, some nodes may not be easily observable at primary outputs. These nodes themselves can be made primary outputs to increase observability, but this is not feasible if there are many unobservable nodes. Alternatively, several unobservable nodes can be consolidated to a single primary output via an XOR tree. The XOR tree, however, requires a lot of space, especially for more complex designs with several pipeline stages, and also increases the number of primary outputs significantly, so this is not very practical.

Alternatively, scannable observation latches can be used where nodes are flagged as unobservable by the ATPG tools in order to increase observability without significantly increasing the primary outputs. The previous methods discussed in[3] improve testability; however, they require significant overhead and still do not provide high fault coverage. For example, the original fault coverage of a 4 × 4 pipelined NCL multiplier was reported to be 16%. After adding XOR gates to the circuit to improve controllability and observability, the fault coverage increased to only 21%. Finally, the insertion of scannable observation latches increased the fault coverage to 45%, which is still not acceptable. In order to cope with low fault coverage, Satagopan etal.[3] then proposed to break the internal feedback path inside every NCL gate and insert a latch. This technique is shown to significantly improve testability (almost 100% fault coverage), but it requires substantial area overhead, which makes it impractical. 2) Synchronous Modeling of NCL Pipeline: The second approach to make the NCL circuits testable, as described in[5], starts with modeling the NCL pipeline and how stuck-at faults impact its behavior. It first proves that in an acyclic NCL pipeline with M stages, the faults in completion detectors can be checked by applying at most M/2 + 1 pairs of {DATA, NULL} to the pipeline. If there is a stuck-at fault at any node inside the completion detectors, the pipeline is guaranteed to stall.

The value of DATA is not important and, in fact, the same DATA value can be repeated. It is further shown that faults in the registers can be eliminated by fault collapsing based on fault dominance. Consequently, both completion detectors and registers can be dropped from stuck-at fault checking. The original NCL pipeline can then be considered as a purely NCL combinational logic, after removing the register and completion detector circuitry. Then proving that irredundant NCL combinational circuits are fully testable for all stuck-at faults, a method is described to generate test vectors using conventional ATPG tools. In this method, each NCL gate is replaced with its set phase equivalent Boolean function. Then, the conventional ATPG tools are used to generate test patterns for all its stuck-at-0 faults, since the NCL circuits are unate and rising transitions only happen during the set phase. The suck-at-1 faults are then checked by padding the generated test vectors with NULL values, because if a DATA value asserts a node in the DATA phase, the following NULL phase will deassert it according to the NCL operation. For cyclic pipelines where there are feedback loops in the datapath, the pipeline needs to be converted to an acyclic pipeline before using the previous method. Partial-scan technique can be used for this purpose.

III. EXISTING MODEL

Fig1 shows the structures of the recently published frequency multipliers that perform better than most previous frequency multipliers [11]. The frequency multiplier in[1] is composed of a D-flip–flop-based pulse generator, a multiplication-ratio control logic, and a push–pull-stagebased edge combiner, as shown in Fig1(a). Owing to its simple edge-combiner structure, this frequency multiplier is suitable for high-frequency multiplied clock generation with low power and a small area. It can also guarantee a 50% duty cycle for its multiplied clock. However, because the output pulses of the pulse generator are generated consecutively [i.e., the kth pulse is generated directly following the (k −1)th pulse], the pulses might overlap owing to process variation or layout mismatch as they pass through the multiplication-ratio control logic; this could cause a short-circuit current to flow in the edge combiner, which in turn could lead to excessive power consumption or malfunction of the frequency multiplier. In addition, the output loading of the edge combiner rapidly increases with the multiplication ratio, because one pull-up pMOS (PU-P) and one pull-down nMOS (PD-N) are added to the output of the edge combiner whenever the maximum multiplication ratio increases by one.

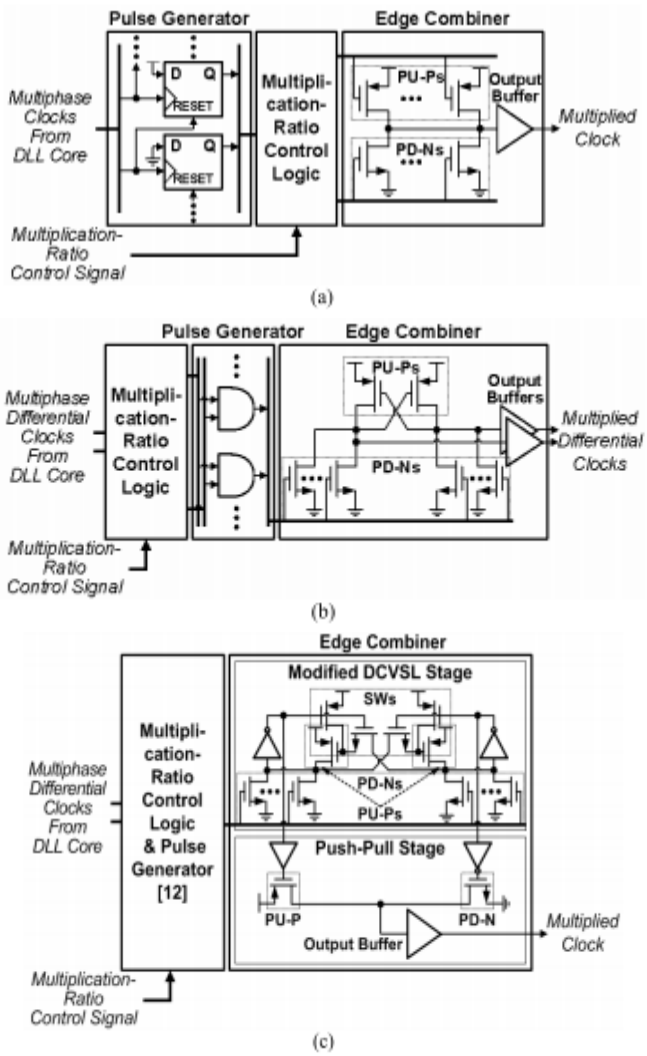

Fig.1. Structure of the frequency multipliers in (a)[1], (b) [2], and (c) [3].

Fig1(b) shows the structure of the frequency multiplier in [12]. This frequency multiplier is composed of a multiplication-ratio control logic, an AND-gate-based pulse generator, and a differential cascade voltage switch (SW) logic (DCVSL)-stage-based edge combiner. The frequency

multiplier can generate the multiplied differential clocks with a small area penalty. As only one PD-N is added to each differential output of the edge combiner when the maximum multiplication ratio is increased by one, the output loading of the edge combiner increases slower than that of the edge combiner in [1]. However, the PD-N should remain on till the positive and the negative edges of the multiplied differential clocks are generated by the edge combiner. In addition, when the PD-N is turned ON, the edge combiner uses a small-sized PU-P to prevent conflict between the PU-P and the PD-N. Because of these restrictions, the frequency multiplier in [2] may not be suitable for high-speed operation and cannot guarantee 50% duty cycle for the multiplied clock. Finally, interphase timing distortion may occur when the multiphase clocks pass through the multiplication-ratio control logic, which in turn can generate pulse overlapping similar to that experienced in the frequency multiplier in [1].

The frequency multiplier in [3] has the same structure as in [2], with the exception that its edge combiner is composed of a modified DCVSL stage and a push–pull stage, as shown in Fig1(c). The modified DCVSL stage has SWs that turn the PU-P OFF when the PD-N is ON, preventing conflict between the PU-P and the PD-N. Therefore, a small-sized PU-P is no longer required; this property efficiently solves the slow operation problem of the DCVSL-stage-based edge combiner in [2]. In addition, by adopting a push–pull stage, 50% duty cycle can be guaranteed for the multiplied clock. Finally, as the modified DCVSL stage maintains the characteristics of a DCVSL structure, only one PD-N is added to each differential output of the modified DCVSL stage when the maximum multiplication ratio is increased by one, as in the edge combiner in [12]. However, the frequency multiplier in [3] still has some problems in common with the frequency multiplier in [1] and [2], including reliability degradation owing to pulse overlapping.

IV. PROPOSED METHOD

As discussed before, each stage of the SCL pipeline is made of four separate blocks: combinational logic function (F_i), completion detector (CD_i), register (R_i), and completion C-element (C_i). Since the stuck-at faults in each block can impact the SCL pipeline in different ways, each block should be analyzed separately.

A. Logic Fault Analysis

1) Faults on Completion C-Element Signals: As mentioned before, the completion C-element is essential to synchronize sleep signals and allow a safe DATA/NULL phase alternation. In addition, the completion C-element is the only gate in the SCL pipeline that does not have sleep capability; hence, it is a normal resettable C-element as used in the NCL logic. A C-element works as follows: the output is asserted when all inputs are asserted; the output remains asserted until all inputs are deasserted (hysteresis behavior). In the SCL, however, this C-element's output is inverted. Since in each DATA/NULL phase all inputs and consequently the output of a completion C-element must make a transition for the corresponding DATA/NULL set to propagate through the pipeline, the following theorem can be deduced.

Theorem 1: In the SCL pipeline, all stuck-at faults on the inputs and output of all completion C-elements can be detected by allowing a single {DATA, NULL} pair to propagate through the pipeline from primary inputs to primary outputs.

Proof: Assume the SCL pipeline is reset to the all-NULL state, where all stages are in sleep mode and the output of all completion C-elements, including the Ki and Ko signals, are high. By providing a single DATA set at the pipeline input, the DATA should propagate all the way through the pipeline and produce a valid DATA set at the pipeline output, only if the inputs and output of all completion C-elements make a single transition each. Once a valid DATA set is detected at the pipeline output, Ki is deasserted and a NULL set is provided at the pipeline input. The NULL set then causes each pipeline stage to consecutively enter the sleep state, which eventually produces a valid NULL set at the pipeline output, only if the inputs and output of completion C-elements make another single transition each. Consequently, a complete propagation of a {DATA, NULL} pair through the pipeline requires that the inputs and output of each completion C-element make exactly one low-to-high and one high-to-low transition or the pipeline stalls (i.e., deadlock state). Therefore, a complete propagation of a {DATA, NULL} pair ensures that there is no stuck-at-0 or stuck-at-1 fault on the inputs and output of completion C-elements. Fig1 shows various signal transitions when a {DATA, NULL} pair propagates through the SCL pipeline.

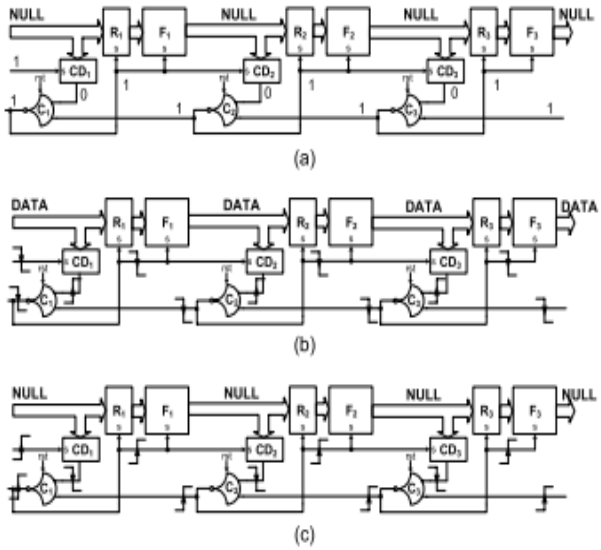

Fig.2. Signal transitions needed for the propagation of a {DATA, NULL} pair. (a) Initial state after reset. (b) DATA propagation. (c) NULL propagation.

2) Faults in Completion Detector: As mentioned before, the stuck-at faults in a completion detector may not necessarily result in a pipeline stall. For example, a stuck-at-1 fault on

the output of any gate in a completion detector (except the final gate) is hidden by the sleep signal. In other words, in NULL phase, even when a gate's output is stuck-at-1, the completion detector will still produce a 0 at its output once the sleep signal is asserted, as long as the output of the last gate in the completion detector is not stuck-at-1. This is in fact a consequence of using the sleep signal to force the completion detector to get cleared rather than requiring the propagation of a NULL wavefront to clear it.

V. RESULTS

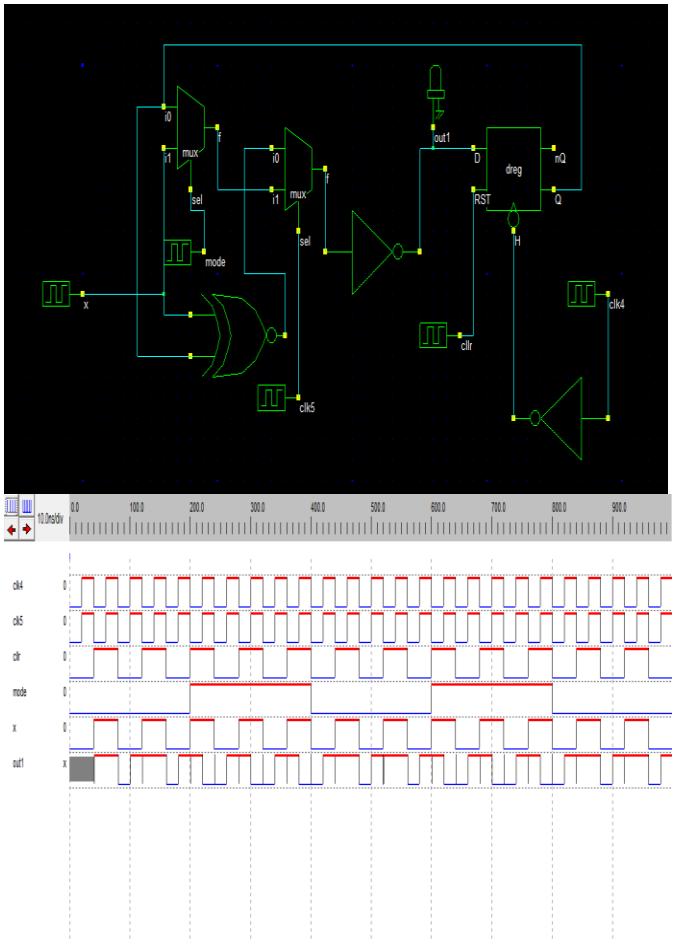

Fig.3. Simulation Results.

VI. CONCLUSION

The problem of testing SCL circuits for stuck-at faults was investigated. The faults were initially divided into two separate categories: 1) faults on logic gates and 2) faults on sleep signal forks. The faults within each category were then analyzed separately, and the impact of the faults inside each SCL component in the SCL pipeline was discussed. A comprehensive scan-based DFT methodology was then proposed based on the fault analysis and the architecture of the scan chain; and the implementation of the scan cells was elaborated. Finally, the proposed DFT methodology was validated through experimental results, showing that the methodology provides a high test coverage (more than 99%) at the cost of the usual area overhead associated with scan chain insertion. Future work consists of exploring other testing techniques, such as delay testing and quiescent current (IDDQ) testing. Since stuck-at faults cannot model all the possible defects in the CMOS technology, other testing techniques are usually used in addition to stuck-at fault testing to increase fault coverage. For example, transistor-level faults that are not covered by the stuck-at fault model, such as bridging faults, stuck-shorts, and stuck-opens, could be potentially tested using IDDQ testing. In addition, in the SCL pipeline, some redundant faults such as the stuck-at-0 faults on the sleep signal forks within a combinational logic block or a completion detector block might be testable using delay testing.

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