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A New Approach for High Speed and Energy Efficient Carry Skip Adder

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Abstract: In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is Achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power, and energy parameters with those of other adders using a 45-nm static CMOS technology for a wide range of supply voltages. The results that are obtained using HSPICE simulations reveal, on average, 44% and 38% improvements in the delay and energy, respectively, compared with those of the Conv-CSKA. In addition, the power–delay product was the lowest among the structures considered in this paper, while its energy–delay product was almost the same as that of the Kogge–Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a reasonably high speed.

Keywords: Carry Skip Adder (CSKA), Energy Efficient, High-Performance,Hybrid Variable Latency Adders, Voltage Scaling.

I. INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALUs) [1] and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in [2]–[9].Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect [10]. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nanoscale technologies. The variations increase uncertainties in the aforesaid performance parameters. In addition, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region [10].

Recently, the near-threshold region has been considered as a region that provides a more desirable tradeoff point between delay and power dissipation compared with that of the sub threshold one, because it results in lower delay compared with the sub threshold region and significantly lowers switching and leakage powers compared with the super threshold region. In addition, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors [11], suffers considerably less from the process and environmental variations compared with the sub threshold region. The dependence of the power (and performance) on the supply voltage has been the motivation for design of circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency) of the circuit based on the workload requirement [12]. For these systems, the circuit should be able to operate under a wide range of supply voltage levels. Of course, achieving higher speeds at lower supply voltages for the computational blocks, with the adders as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors. In addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays, power consumptions, and area usages.

Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures along with their characteristics may be found in [1] and [13]. The RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA. The PPAs, which are also called carry look-ahead adders, exploit direct parallel prefix structures to generate the carry as fast as possible [14]. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, the Kogge–Stone adder (KSA) [15] is one of the fastest structures but results in large power consumption and area usage. It should be noted that the structure complexities of PPAs are more than those of other adder schemes [13], [16]. The CSKA, which is an efficient adder in terms of power consumption and area usage, was introduced in [17]. The critical path delay of the CSKA is much smaller than the one in the RCA, whereas its area and power consumption are similar to those of the RCA. In addition, the power-delay product (PDP) of the CSKA is smaller than those of the CSLA and PPA structures [19]. In addition, due to the small number of transistors, the CSKA benefits from relatively short wiring lengths as well as a regular and simple layout [18]. The comparatively lower speed of this adder structure, however, limits its use for high-speed applications.

In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic. The concentration on the static CMOS originates from the desire to have a reliably operating circuit under a wide range of supply voltages in highly scaled technologies [10]. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, the design of (hybrid) variable latency CSKA structures have been reported in the literature. Hence, the contributions of this paper can be summarized as follows.

- Proposing a modified CSKA structure by combining the concatenation and the incrementation schemes to the conventional CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer.
- Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay.
- Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure (from the nominal supply voltage to the near-threshold voltage).
- Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with a PPA, which is modified in this paper.

The rest of this paper is organized as follows. Section II discusses related work on modifying the CSKA structure for improving the speed as well as prior work that use variable latency structures for increasing the efficiency of adders at low supply voltages. In Section III, the Conv-CSKA with fixed stage size (FSS) and variable stage size (VSS) is explained, while Section IV describes the proposed static CSKA structure. The hybrid variable latency CSKA structure is suggested in Section V. The results of comparing the characteristics of the proposed structures with those of other adders are discussed in Section VI. Finally, the conclusion is drawn in Section VII.

II. PRIOR WORK

Since the focus of this paper is on the CSKA structure, first the related work to this adder are reviewed and then the variable latency adder structures are discussed.

A. Modifying CSKAs for Improving Speed

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures [19]. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder [23]. Many methods have been suggested for finding the optimum number of the FAs [18]–[26]. The techniques presented in [19]–[24] make use of VSSs to minimize the delay of adders based on a single level carry skip logic. In [25], some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause area and power increase considerably and less regular layout. The design of a static CMOS CSKA where the stages of the CSKA have a variable sizes was suggested in [18]. In addition, to lower the propagation delay of the adder, in each stage, the carry look-ahead logics were utilized.

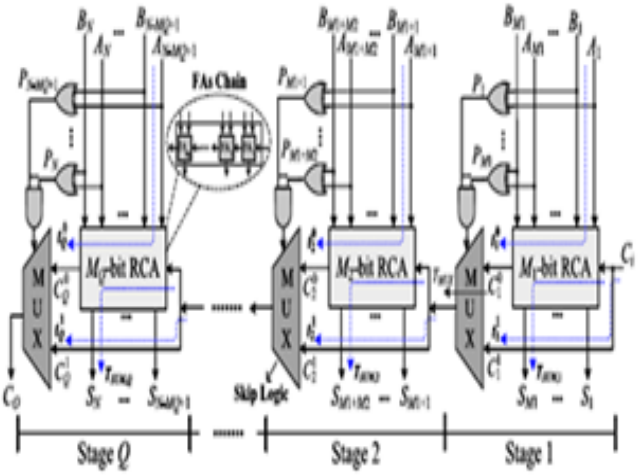

Fig.1. Conventional Structure Of The CSKA.

Again, it had a complex layout as well as large power consumption and area usage. In addition, the design approach, only for the 32-bit adder, was not general to be applied for structures with different bits lengths. Alioto and Palumbo [19] propose a simple strategy for the design of a single-level CSKA. The method is based on the VSS technique where the near-optimal numbers of the FAs are Determined based on the skip time (delay of the multiplexer), and the ripple time (the time required by a carry to ripple through a FA). The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio [17], [20]. In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. Even for the speed, the delay of skip logics, which are based on multiplexers and form a large part of the adder critical path delay [19], has not been reduced.

B. Improving Efficiency of Adders at Low Supply Voltages

To improve the performance of the adder structures at low supply voltage levels, some methods have been proposed in [27]–[36]. In [27]–[29], an adaptive clock stretching operation has been suggested. The method is based on the Observation that the critical paths in adder units are rarely activated. Therefore, the slack time between the critical paths and the off-critical paths may be used to reduce the supply voltage. Notice that the voltage reduction must not increase the delays of the noncritical timing paths to become larger than the period of the clock allowing us to keep the original clock frequency at a reduced supply voltage level. When the critical timing paths in the adder are activated, the structure uses two clock cycles to complete the operation. This way the power consumption reduces considerably at the cost of Rather small throughput degradation. In [27], the efficiency of this method for reducing the power consumption of the RCA structure has been demonstrated. The CSLA structure in [28] was enhanced to use adaptive clock stretching operation where the enhanced structure was called cascade CSLA (C2SLA). Compared with the common CSLA structure, C2SLA uses more and different sizes of RCA blocks. Since the slack time between the critical timing paths and the longest off-critical path was small, the supply voltage scaling, and hence, the power reduction were limited. Finally, using the hybrid structure to improve the effectiveness of the adaptive clock stretching operation has been investigated in [31] and [33]. In the proposed hybrid structure, the KSA has been used in the middle part of the C2SLA where this combination leads to the positive slack time increase. However, the C2SLA and its hybrid version are not good candidates for low-power ALUs. This statement originates from the fact that due to the logic duplication in this type of adders, the power consumption and also the PDP are still high even at low supply voltages [33].

III. CONVENTIONAL CARRY SKIP ADDER

The structure of an N-bit Conv-CSKA, which is based on blocks of the RCA (RCA blocks), is shown in Fig. 1. In addition to the chain of FAs in each stage, there is carry skip logic. For an RCA that contains N cascaded FAs, the worst propagation delay of the summation of two N-bit Numbers, A and B, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where

$$P_i = A_i \oplus B_i = 1 \quad \text{for } i = 1, \ldots, N \tag{1}$$

Where P_i is the propagation signal related to A_i and B_i. This shows that the delay of the RCA is linearly related to N [1].In the case, where a group of cascaded FAs are in the propagate mode, the carry output of the chain is equal to the carry input.

In the CSKA, the carry skip logic detects this situation, and makes the carry ready for the next stage without waiting for the Operation of the FA chain to be completed. The skip operations performed using the gates and the multiplexer shown in the figure. Based on this explanation, the N FAs of the CSKA are grouped in Q stages. Each stage contains an RCA block with M_j FAs (j = 1, . . . , Q) and a skip logic. In each stage, the inputs of the multiplexer (skip logic) are the carry input of the stage and the carry output of its RCA block (FA chain).In addition, the product of the propagation signals (P) of the stage is used as the selector signal of the multiplexer. The CSKA may be implemented using FSS and VSS where the highest speed may be obtained for the VSS structure [19], [22]. Here, the stage size is the same as the RCA block size. In Sections III-A and III-B, these two different implementations of the CSKA adder are described in more detail.

A. Fixed Stage Size CSKA

By assuming that each stage of the CSKA contains M FAs, there are Q = N/M stages where for the sake of simplicity, we assume Q is an integer. The input signals of the j^{th} multiplexer are the carry output of the FAs chain in the j^{th} stage denoted by C_{0j}, the carry output of the previous stage(carry input of the j^{th} stage) denoted by C_{1j} (Fig. 1). The critical path of the CSKA contains three parts: 1) the path of the FA chain of the first stage whose delay is equal to M × TCARRY; 2) the path of the intermediate carry skip multiplexer whose delay is equal to the (Q – 1)× TMUX; and3) the path of the FA chain in the last stage whose its delay is equal to the (M −1) × TCARRY +TSUM. Note that TCARRY,TSUM, and TMUX are the propagation delays of the carry output of an FA, the sum output of an FA, and the output delay of a2:1 multiplexer, respectively. Hence, the critical path delay of a FSS CSKA is formulated by

$$T_D = [M \times T_{\text{CARRY}}] + \left[\left(\frac{N}{M} - 1\right) \times T_{\text{MUX}}\right] + [(M-1) \times T_{\text{CARRY}} + T_{\text{SUM}}]. \tag{2}$$

Based on (1), the optimum value of M (Mopt) that leads to optimum propagation delay may be calculated as (0.5Nα)1/2where α is equal to TMUX/TCARRY. Therefore, the optimum propagation delay (TD,opt) is obtained from

$$T_{D,\text{opt}} = 2\sqrt{2NT_{\text{CARRY}}T_{\text{MUX}}} + (T_{\text{SUM}} - T_{\text{CARRY}} - T_{\text{MUX}}) = T_{\text{SUM}} + (2\sqrt{2N\alpha} - 1 - \alpha) \times T_{\text{CARRY}}. \tag{3}$$

Thus, the optimum delay of the FSS CSKA is almost proportional to the square root of the product of N and α [19].

B. Variable Stage Size CSKA

As mentioned before, by assigning variable sizes to the stages, the speed of the CSKA may be improved. The speed improvement in this type is achieved by lowering the delays of the first and third terms in (1). These delays are minimized by lowering sizes of first and last RCA blocks. For instance, the first RCA block size may be set to one, whereas sizes of the following blocks may increase. To determine the rate of increase, let us express the propagation delay of the C_{1j} (t_{1j}) by

$$t_j^1 = \max\left(t_{j-1}^0, t_{j-1}^1\right) + T_{\mathrm{MUX}} \quad (4)$$

Where $t0_{j-1}$ (t^1_{j-1}) shows the calculating delay of C^0_{j-1}(C^1_{j-1})signal in the (j − 1)th stage. In a FSS CSKA, except in the first stage, t0jis smaller than t^1j. Hence, based on (3), the delay of $t0_{j-1}$ may be increased from t^0_1 to t^1_{j-1} without increasing the delay of C^1_j signal. This means that one could increase the size of the (j − 1)th stage (i.e., Mj−1) without increasing the propagation delay of the CSKA. Therefore, increasing the size of M_i for the j th stage should be bounded by

$$t_j^0 \le t_j^1 = t_1^0 + (j-1)T_{\mathrm{MUX}}. \quad (5)$$

Since the last RCA block size also should be minimized, the increase in the stage size may not be continued to the last RCA block. Thus, we justify the decrease in the RCA block sizes toward the last stage. First, note that based on Fig. 1, the output of the j^{th} stage is, in the worst case, accessible aftert1j+ TSUM, j. Assuming that the p^{th} stage has the maximum RCA block size, we wish to keep the delay of the outputs of the following stages to be equal to the delay of the output of the p^{th} stage. To keep the same worst case delay for the critical path, we should reduce the size of the following RCA blocks. For example, when i ≥ p, for the $(i+1)^{th}$ stage, the output delay is t_1I + TMUX + TSUM,i+1, where TSUM,i+1 is the delay of the $(i+1)^{th}$ RCA block for calculating all of its sum outputs when its carry input is ready. Therefore, the size of the $(i+1)^{th}$ stage should be reduced to decrease TSUM,i+1preventing the increase in the worst case delay (TD) of the adder. In other words, we eliminate the increase in the delay of the next stage due to the additional multiplexer by reducing the sum delay of the RCA block. This may be analytically expressed as

$$T_{\mathrm{SUM},i+1} \le T_{\mathrm{SUM},i} - T_{\mathrm{MUX}}; \quad \text{for } i \ge p \quad (6)$$

The trend of decreasing the stage size should be continued until we produce the required number of adder bits. Note that, in this case, the size of the last RCA block may only be one (i.e., one FA). Hence, to reach the highest number of input bits under a constant propagation delay, both (4) and (5) should be satisfied. Having these constraints, we can minimize the delay of the CSKA for a given number of input bits to find the stages sizes for an optimal structure. In this optimal CSKA, the size of first p stages is increased, while the size of the last (Q− p) stages is decreased. For this structure, the p^{th} stage, which is called nucleus of the adder, has the maximum size [24].Now, let us find the constraints used for determining the optimum structure in this case. As mentioned before, when the j^{th} stage is not in the propagate mode, the carry output of the stage is C^0_j. In this case, the maximum of t^0_j is equal to M_j × TCARRY. To satisfy (4), we increase the size of the first p stages up to the nucleus using [19]

$$M_j \le M_1 + (j-1)\alpha; \quad \text{for } 1 \le j \le p \quad (7)$$

In addition, the maximum of TSUM,i is equal to (M_i −1)×TCARRY + TSUM. To satisfy (5), the size of the last (Q − p) stages from the nucleus to the last stage should decrease based on [19]

$$M_i \ge M_Q + (Q-i)\alpha; \quad \text{for } p \le i \le Q. \quad (8)$$

In the case, where α is an integer value, the exact sizes of stages for the optimal structure can be determined. Subsequently, the optimal values of M1, MQ, and Q as well as the delay of the optimal CSKA may be calculated [19]. In the case, where α is a no integer value, one may realize only a near optimal structure, as detailed in [19] and [21]. In this case, most of the time, by setting M_1 to 1 and using (6) and (7),the near-optimal structure is determined. It should be noted that, in practice, α is non integer whose value is smaller than one. This is the case that has been studied in [19], where the estimation of the near-optimal propagation delay of the CSKA is given by [19]

$$T_{D,\mathrm{opt}} = \left(2\left\lceil\frac{\alpha}{2}\right\rceil - 1\right)T_{\mathrm{CARRY}} + \left(2\sqrt{\frac{N}{\alpha}} - 1\right)T_{\mathrm{MUX}} + T_{\mathrm{SUM}}. \quad (9)$$

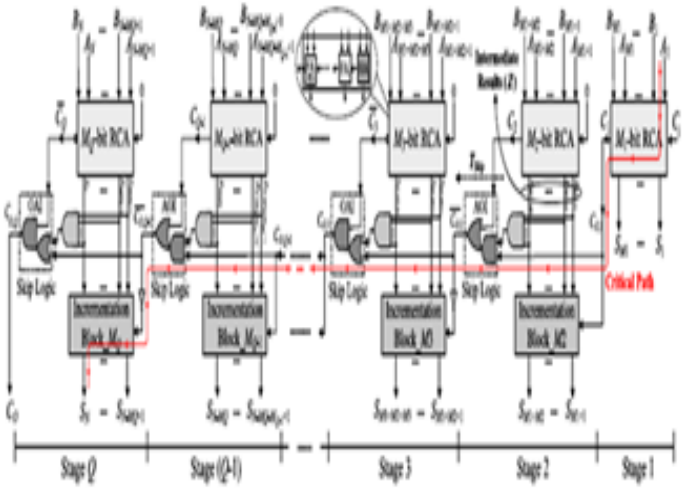

Fig.2. Proposed CI-CSKA Structure.

This equation may be written in a more general Formby replacing TMUX by TSKIP to allow for other logic types instead of the multiplexer. For this form, α becomes equal to TSKIP/TCARRY. Finally, note that in real implementations, SKIP < TCARRY, and hence, α/2 becomes equal to one. Thus, (8) may be written as

$$T_{\mathrm{PD_{opt}}} = T_{\mathrm{CARRY}} + \left(2\sqrt{\frac{N}{\alpha}} - 1\right)T_{\mathrm{SKIP}} + T_{\mathrm{SUM}}. \quad (10)$$

Note that, as (9) reveals that a large portion of the critical path delay is due to the carry skip logics.

IV. PROPOSED CSKA STRUCTURE

Based on the discussion presented in Section III, it is concluded that by reducing the delay of the skip logic, one may lower the propagation delay of the CSKA significantly. Hence, in this paper, we present a modified CSKA structure that reduces this delay as shown in Fig.2.

V. IMPLEMENTATION RESULTS

Results of this paper is as shown in bellow Figs.3 to 5.

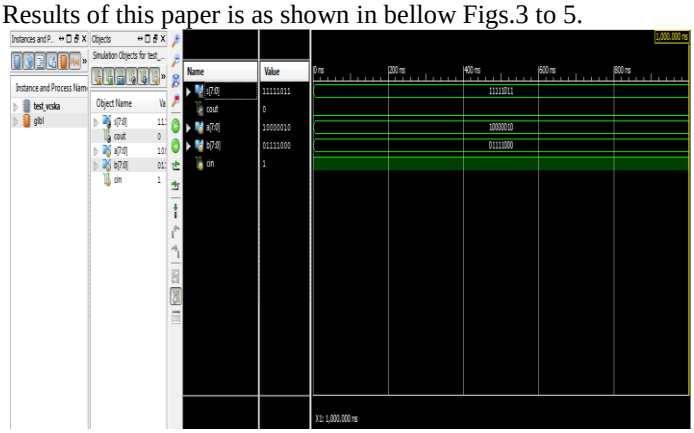

Fig.3. simulation result for the proposed system.

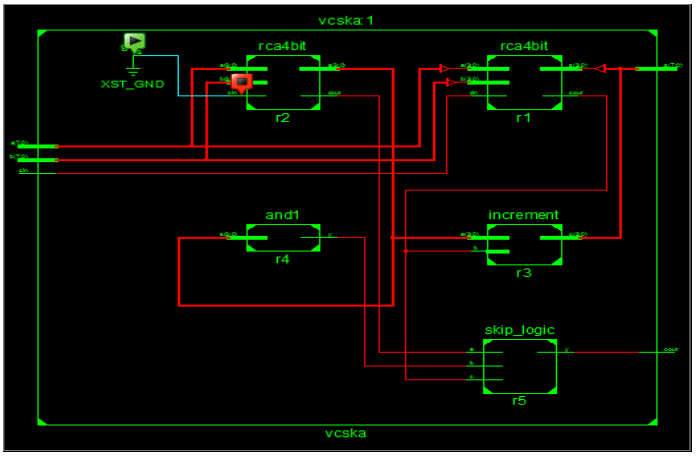

Fig.4. RTL schematic view for the proposed system.

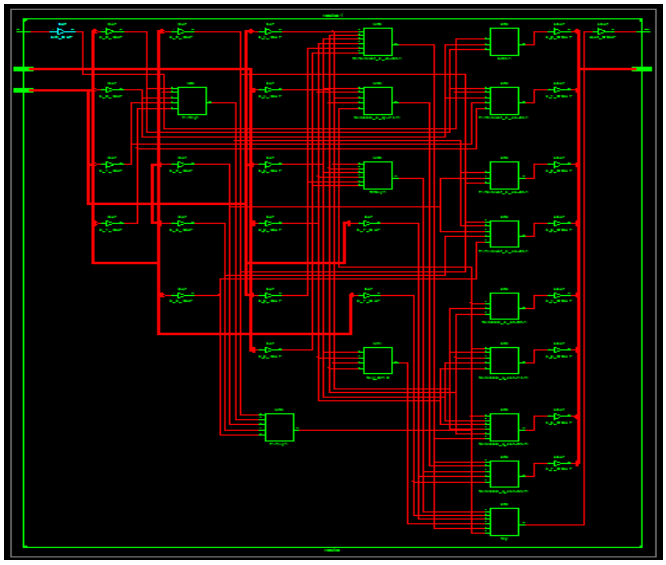

Fig.5. Technology schematic view for the proposed system.

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