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A Novel approach of a Z-Source Ultra sparse Matrix Converter in Buck and Boost Modes of Operation

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Abstract: In this project an in-depth study on the operation and control of the ZSUSMC in buck and boost modes is conducted. An optimal SP that results in minimum number of changes in the switching states is proposed. Two space vector modulation schemes, with and without a zero state in the rectifier stage modulation, are presented and their advantages and disadvantages are discussed. In addition, restrictions imposed on the converter operation in buck mode, which arise from unidirectional nature of the ultra- sparse matrix converter, are discussed and a solution is proposed for offsetting those limitations. Furthermore, an optimal switching pattern, which results in minimum pos- sible number of changes in the switching states as well as even distribution of the shoot-through state over the entire control period, is proposed. Also, common-mode voltages of the converter in all possible switching configurations are calculated. Hardware-in-the-loop studies of a ZSUSMC- based permanent magnet synchronous motor drive are car- ried out to evaluate the performance of the drive under the proposed modulation techniques. The obtained results are compared with a recent study and the superiority of the pro- posed method in terms of converter input/output current quality is demonstrated.

Keywords: Buck Mode, Switching Pattern (SP), Space Vector Modulation (SVM), Ultrasparse Matrix Converter (USMC), Z-Source (ZS).

I. INTRODUCTION

A discretionary number of input lines can be associated with a subjective number of output lines specifically utilizing bidirectional semiconductor switches. The various transformation stages and energy storage components of conventional inverter and cycloconverter circuits can be replaced by one exchanging network. A matrix converter is an ac to ac converter prepared to do specifically changing over an ac power supply voltage into an ac voltage of variable amplitude and frequency without a huge energy storage element [1]. The principal portrayal of a matrix converter was distributed in 1976 by Gyugyi and Pelly [2]. In 1980,Venturini and Alesina exhibited the first calculation fit for incorporating output sinusoidal reference voltages[1]. Late research on matrix converters has concentrated for the most part on modulation plans [3]-[8] and on drive applications. Clearly, all distributed studies have managed mostly with three-stage circuit topologies. The principal investigation of a solitary stage matrix converter was performed by Zuckerberger et al. [9] on a frequency step-up and elementary voltage step-down converter. Utilisation of single-phase matrix converters has been portrayed for induction motor drives, radio-frequency induction heating, audio power amplification, and compensation voltage sags and swells. It has been accounted for that the use of safe-commutation switches with pulse width modulation (PWM) control can essentially enhance the performance of ac/ac converters. However, in the conventional single-phase matrix converter topology [9]-[13],the ac output voltage cannot exceed the ac input voltage. Furthermore, it is unacceptable to show both two-way switches of one phase leg on at the same time; otherwise, the current spikes generated by this action will destroy the switches. These drawbacks can be overcome by using Z-source topology [14].

Research on Z-source converters has centered primarily on dc/ac inverters and ac/ac converters. The Z-source ac/ac converters focus on single- phase topologies [15]-[17] and three-phase topologies. In applications where solely voltage regulation is required, the group of single-phase Z-source ac/ac converters proposed in [15]-[17] has a variety of deserves, such as providing a bigger range of output voltages with the buck-boost mode, reducing inrush, and harmonic current. However, no one has designed a device primarily based on a Z-source structure and a matrix converter topology that can offer ac/ac power conversion with each a variable output voltage and a step-changed frequency. Here, we apply the Z-source thought to a single- phase matrix converter to produce a new kind of device known as a single-phase Z-source buck-boost matrix converter. This single-phase Z-source buck-boost matrix converter will offer a wide vary of output ac voltages in buck-boost mode with step-down/step-up frequencies. It is shown from operational principles, analyses and simulation that this single-phase Z-source buck-boost matrix converter will buck and boost voltages in step-down/step-up frequency operation. A safe-commutation technique that is very straightforward to implement as a free-wheeling path to provide the needed free-wheeling operation just like what's offered in alternative device topologies is used. The safe- commutation scheme sets up a persistent current way in dead time to wipe out voltage spikes on switches without a snubber circuit.

II. LITERATURE SURVEY

A. Basic Matrix Converter(MC) Topologies

Broadly,the existing frequency converter designs can be classified into 2 categories: direct and indirect converters. To reduce number of switches in the conventional matrix converter, major step was taken with regard to the further development of matrix converter topologies which occurred in 2001 as Indirect matrix converter topologies known as Sparse Matrix Converters as shown in Fig.1 by Kolar et al followed by the first experimental results of a Very Sparse Matrix Converter (Fig.2). Ziegler et al in 2004 advocated possible circuit topologies referred as S-A-X converters.

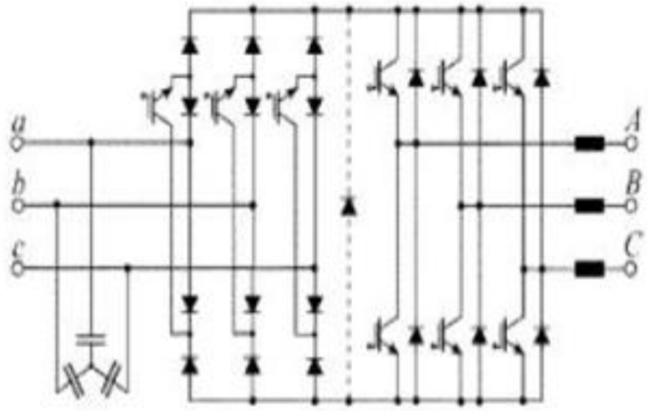

Fig1. Sparse Matrix Converter.

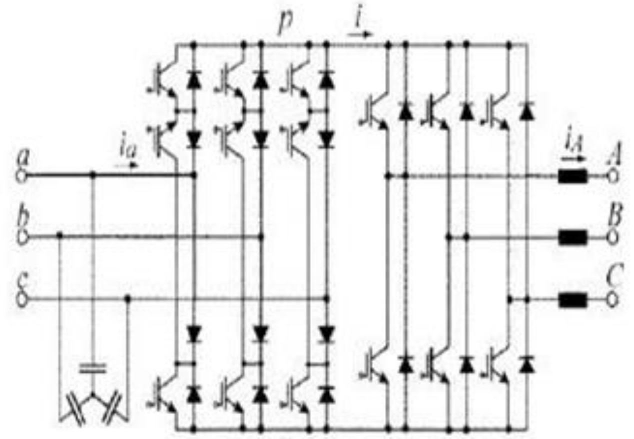

Fig2.Very Sparse Matrix Converter.

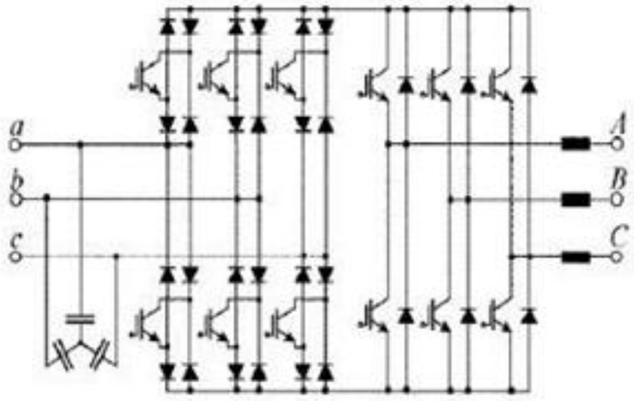

Fig3. Ultra Sparse Matrix Converter.

The same concept was proposed in 2002 by Kolar et al for the Sparse Matrix Converters known as Ultra Sparse Matrix Converter as shown in(Fig3). The ultra-sparse matrix converter (USMC), shown in Fig.3, is the most simple form of the IMC, comprising only 9 individual switches and 18 diodes. The Ultra Sparse MC itself is a variant of the sparse matrix converter (SMC), shown in Fig.1. The USMC and SMC operate by creating a dc link,with the input stage and by using the output stage to provide inversion. The main variation between the IMC and SMC is that the USMC only permits unidirectional power flow due to the arrangement of the input switches.

B. Single phase Matrix Converter(MC) Topologies

Fig4(a) and (b) shows a single-phase Z-source, PWM voltage-fed, buck-boost converter and current-fed buck-boost converter, respectively. The output voltage of the proposed ac-ac converter can be bucked or boosted by controlling the duty ratio D. In addition, the output voltage can be in-phase or out-of-phase with the input voltage depending on operating regions. This is a unique feature of the Z-source converter [16]

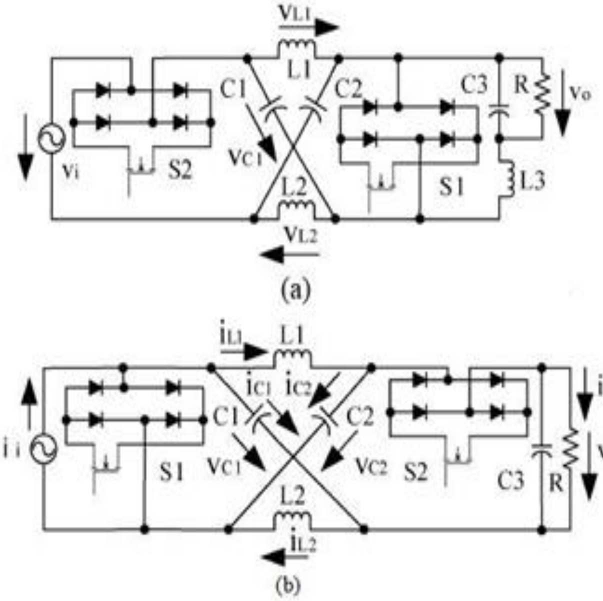

Fig 4. Single-phase Z-source ac-ac converter:(a)voltage-fed and (b)currentfed topologies.

A true bi-directional switch must be realized by the combination of conventional unidirectional semiconductor devices. Fig.5.shows diverse bi-directional switch setups which have been utilized as a part of model and/or proposed in Another problem, tightly related to the bi-directional switches implementation is the commutation problem. The absence of static freewheeling paths gives rise to commutation issues . As a consequence it becomes a difficult task to safely commutate the current, since a particular care is required in the timing and synchronisation of the switches command signals.

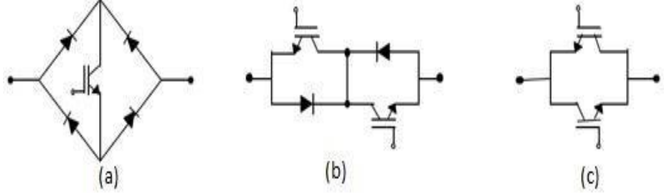

Fig.5.Basic input filter configurations used in matrix converter prototypes(.a)Capacitors star or delta connected. (b)Second order L-C filter (c)L-C filter with parallel damping resistor.

C. The input filter

The input filter design for static power converters operating from an ac power system has to meet three main requirements:

1. carry out the required switching noise attenuation;
2. having a low input displacement angle between filter input voltage and current;
3. guaranty overall system stability.

In addition to these requirements, a set of considerations related to cost, system efficiency, voltage attenuation, and filter parameter variation have to be made for an optimized input filter design [21], [22].

III.PROPOSED SWITCHING PATTERN

Although some SPs for ZSIMC are proposed in the literature, they are not optimal or do not lead to sinusoidal input and output quantities, and consequently, further improvements can be achieved. The proposed SP in this paper results in minimum possible number of changes in the switching states of the converter as well as even distribution of the shoot-through state over the entire control period. The proposed SP for modulation scheme with a zero state in SVR is summarized in Table III. For the modulation scheme without a zero state in SVR, only the last eight subdurations (under di1 and di2) must be considered. By examining (2), one can see that when the space vector of input current reference is at the beginning of a sector, di1 is at its maximum and di2 is zero. When this vector rotates within the sector, di1 gradually decreases and di2 increases such that at the middle of the sector, they become equal. This issue would deteriorate the current modulation if the sector of the input current vector at the kth and (k 1)th samples (two consecutive samples) is different. In order to understand this issue better, consider Fig. 5(a). The figure shows the gate signal associated with the shoot-through state during three consecutive control periods under the condition that modulation without the zero state in SVR is adopted and the vector of input current reference is at an odd-number rectifier sector. Furthermore, in order to minimize the number of switching instants when transitioning from an active state to the zero state (111), the sequence of the inverter active states changes depending on the sector of the output voltage vector. Following the proposed pattern, the number of switching transitions in the rectifier stage over one switching period is two and three without and with a zero state in SVR, respectively. Also, the maximum number of changes in the state of each inverter switch over a switching period is two and three for modulation schemes without and with a zero state in SVR, respectively.

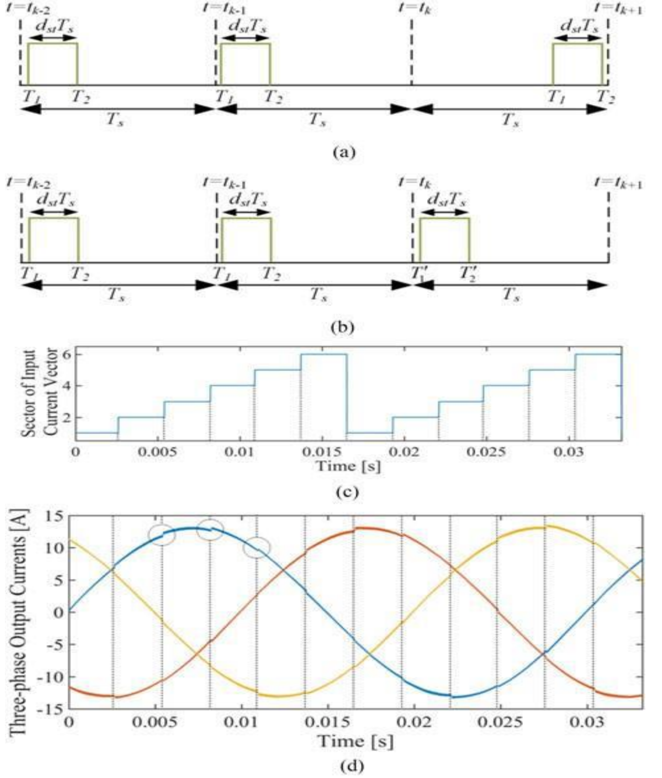

Fig. 5. Gate signals associated with the shoot-through state. (a) Conventional SP, (b) proposed SP, (c) sector of the input current vector, and (d) three-phase output currents without the change in the sequence of d_{i1} and d_{i2}.

IV. SIMU:ATION RESULTS

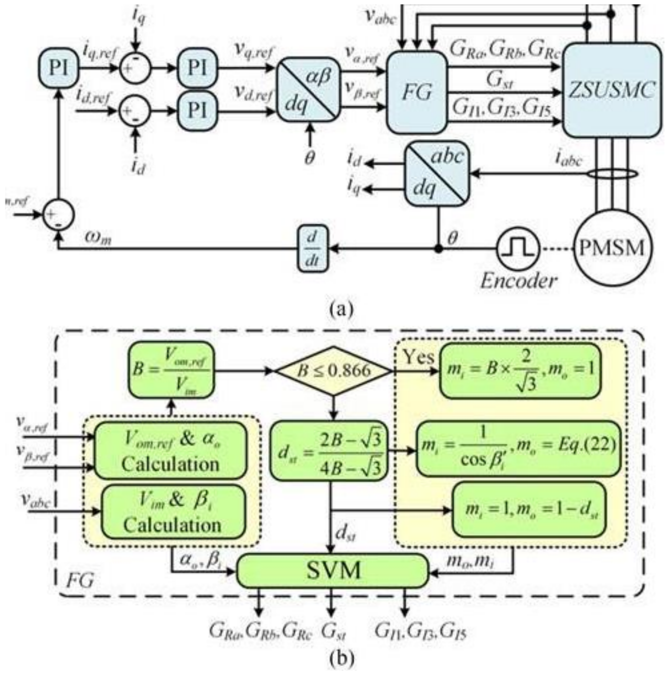

Fig6. (a) Control block diagram of a ZSUSMC-based PMSM drive, (b) details of the function generator (FG).

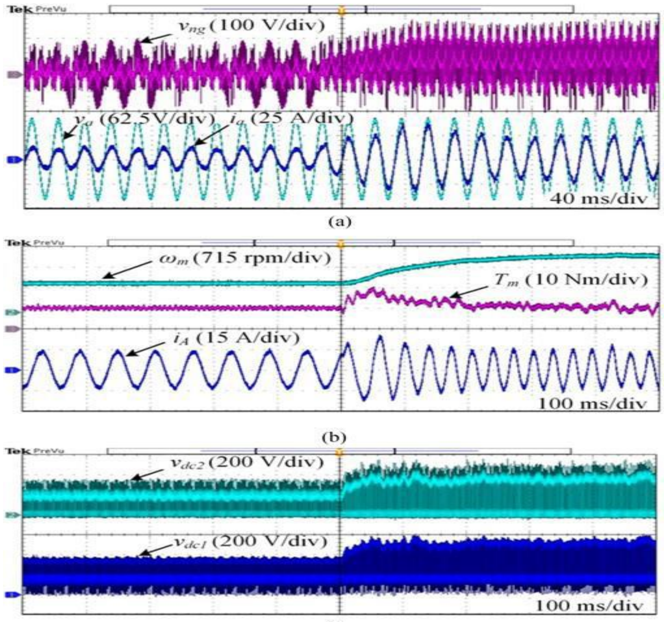

Fig7. SVM with a zero state in SVR with a step change in reference speed from 1000to 2000 r/min. (a) CMV, input voltage, and input current; (b) motor speed, torque, and stator current; and (c) v_{dc1} and v_{dc}2.

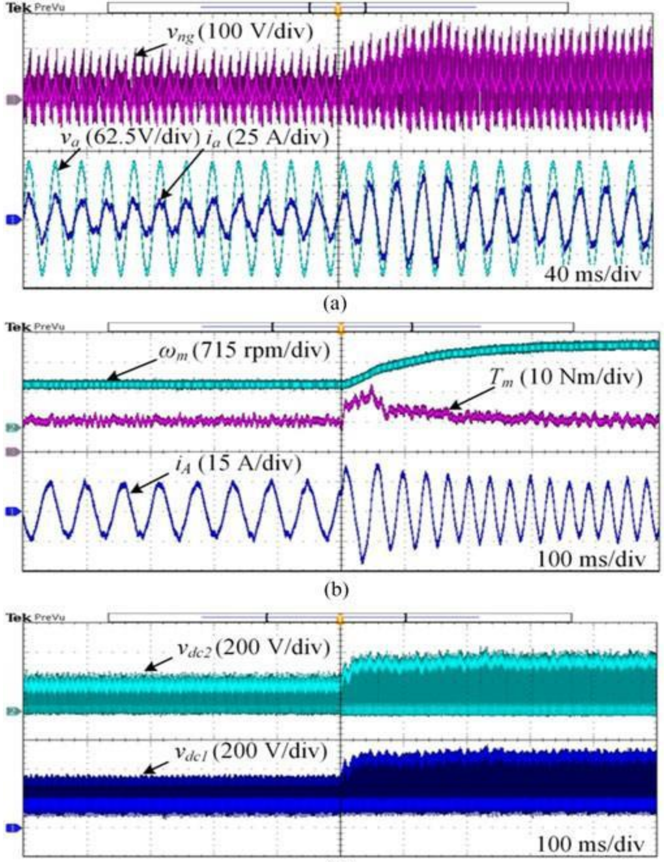

Fig. 8. SVM proposed in [25] without a zero state in SVR with a step change in reference speed from 1000 to 2000 r/min. (a) CMV, input voltage, and input current; (b) motor speed, torque, and stator current; and (c) v_{dc1} and v_{dc2}.

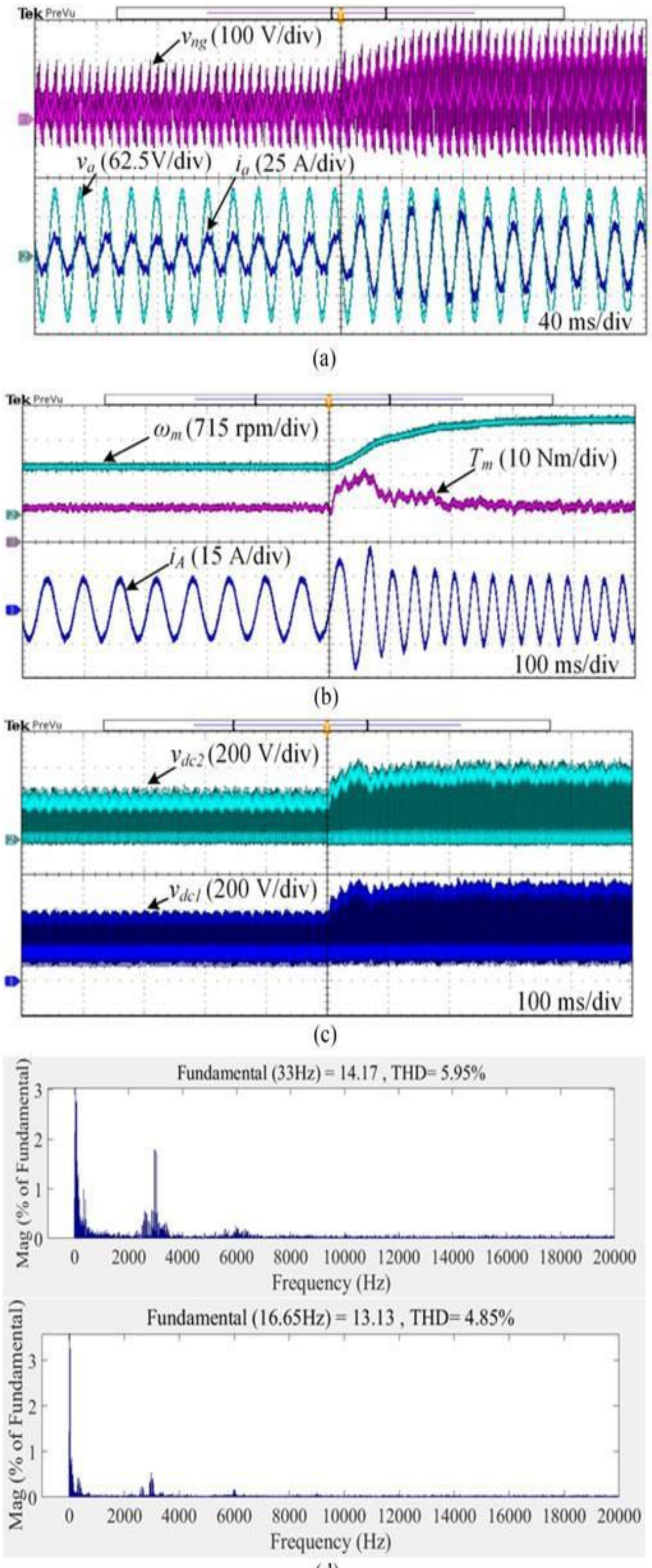

Fig. 9. Proposed SVM without a zero state in SVR with a step change in reference speed from 1000 to 2000 r/min. (a) CMV, input voltage, and input current; (b) motor speed, torque, and stator current; (c) v_{dc1} and v_{dc2} ; and (d) FFT of stator current at 1000 and 2000 r/min (from top to bottom).

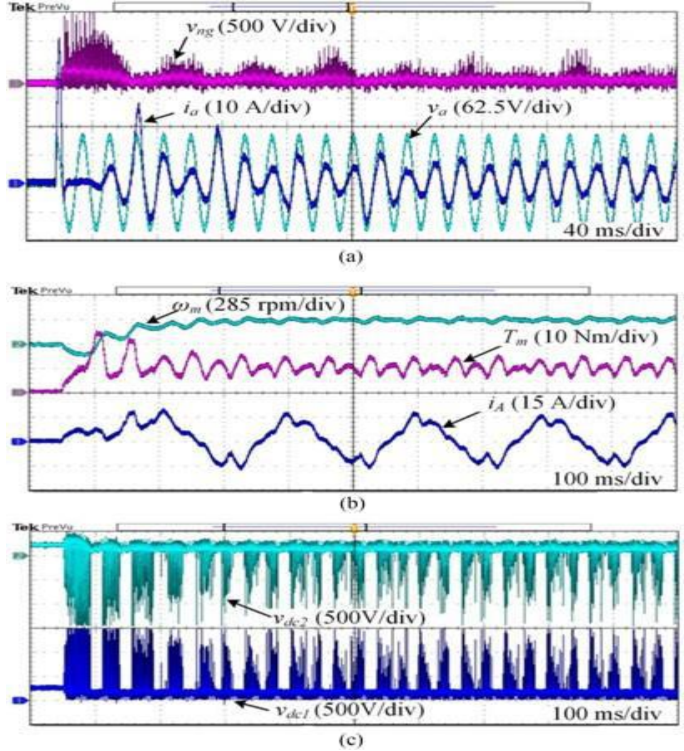

Fig10. Buck mode (mi = 1 and mo is variable) with a step change in reference speed from 0 to 300 r/min. (a) CMV, input voltage, and current;(b) motor speed, torque, and stator current; and (c) v_{dc1} and v_{dc2}.

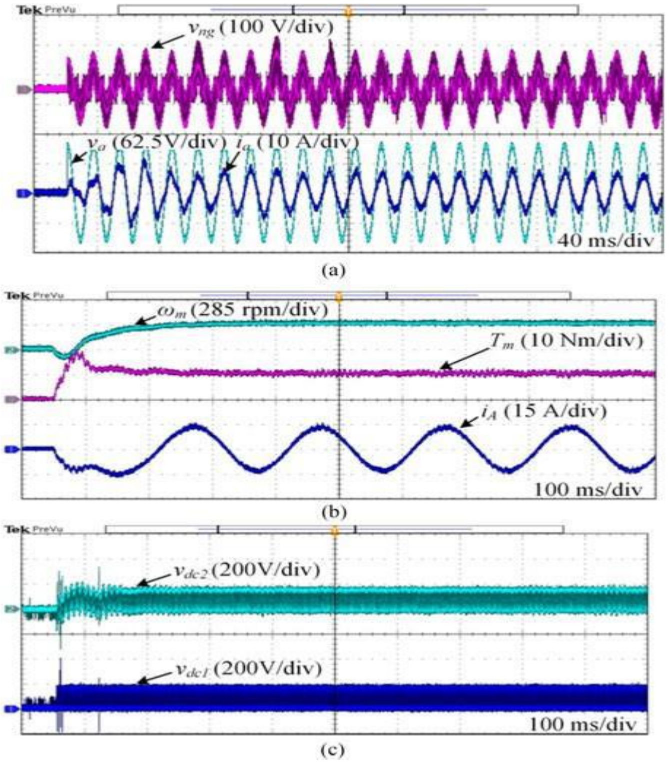

Fig. 11. Buck mode (mo = 1 and mi is variable) with a step change in reference speed from 0 to 300 r/min. (a) CMV, input voltage, and current;(b) motor speed, torque, and stator current; and (c) v_{dc1} and v_{dc2}.

V. CONCLUSION

Two modulation schemes for ZSUSMC with and without a zero state in SVR were proposed. A novel SP, which resulted in reduced number of changes in the switching transitions, was developed. Furthermore, CMV of the converter in all possible switching configurations of the rectifier and inverter stages was obtained. It was demonstrated that the converter con- trolled under the modulation scheme with a zero state in SVR drew/generated sinusoidal input currents/output voltages. How- ever, it was highly complex to implement and had high switching loss. The modulation scheme without a zero state in SVR resulted in sinusoidal output voltages and was less complex. However, the converter drew distorted input currents under this modulation scheme. In addition, it was concluded that due to the unidirectional nature of the USMC topology, a discontinuous inductor current operation mode can occur. A solution was pro- posed for avoiding the converter operation in this mode.

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