IP CORE GENERATION OF DIRECT DIGITAL SYNTHESIZER

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***ABSTRACT*: -** *A harmonic signal generator with adjustable harmonic proportion, phase and frequency is designed in this. The design of this harmonic signal generator is based on direct digital frequency synthesis (DDS) technology and the idea of System on a Programmable Chip (SOPC). The classic structure of DDS is introduced and a kind of compression ROM is designed. The DDS core with compression ROM is compiled using ISE Simulator by VHDL language. A kind of processor which is supplied by xilinx, the soft core, Nois II is embedded on FPGA chip. Using SPARTAN 3E, a system is designed on one single FPGA chip. The performances as expansibility and integration are very much improved. The optimized structure of DDS core and the design SOPC on single FPGA are presented.*

Key words: *DDFs, Phase Accumulator, Xilinx, Spartan3e*

1. INTRODUCTION

Direct Digital Synthesis (DDS) is an electronic method for digitally creating arbitrary waveforms and frequencies from a single, fixed source frequency. With the development of VLSI technology and the requirement of modern communication systems, direct digital frequency synthesizers have been widely used in wireless transceivers since the 1980's. Direct Digital Frequency Synthesis (simply DDS or DDFS), it also known as Numerically Controlled Oscillator (NCO), is a technique which uses digital-data and mixed/analog-signal processing blocks as a means to generate signal waveforms that are repetitive in nature. A DDFS can achieve fast frequency switching in small frequency steps, over a wide band. It provides linear phase and frequency shifting with good spectral purity. A DDFS is used especially for a precise, high frequency and a phase tunable output. A standard DDFS architecture consists of an accumulator, a ROM /lookup table, a DAC and some reconstruction filters.

DDFS solutions are implemented in LSI (large-scale integration) and they play an ever increasing role in digital waveform and clock generation, and modulation. A major advantage of a direct digital synthesizer (DDS) is phase, output frequency and amplitude can be precisely and rapidly manipulated under digital processor control.

Other inherent DDFS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly "hop" between frequencies.

It is easy to include different modulation capabilities in the DDFS by using digital signal processing methods, as the signal is in digital form. By programming the DDFS, modulation formats, adaptive channel bandwidths, frequency hopping and data rates are achieved. The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. The DDFS addresses a variety of applications, as measurement equipments, arbitrary waveform generators, cellular base stations, cable modems and wireless local loop base stations.

1.2 DDFS Overview

Direct digital frequency synthesis (DDFS) is a method of producing an analog waveform, which is a sine wave with a time-varying signal in digital form and then performing a digital-to-analog conversion. The operations within a DDFS device are primarily digital therefore; it can offer fast switching between fine frequency resolution, output frequencies, and operation over a broad spectrum of frequencies.

The digital frequency synthesis approach employs a stable source frequency i.e. reference clock to define times at which digital sinusoidal sample values are produced. These samples are converted from digital to analog format and smoothed by reconstruction filter to produce analog frequency signals. A DDFS typically consists of a phase accumulator (PA) and a sine lookup table (LUT). The input to the phase accumulator is a frequency control, determines the periodicity of the phase accumulator. The PA is updated to the frequency control word or tuning word, at each clock, the output of the PA is fed to LUT. The output of LUT is converted to an analog signal using a digital to analog converter.

The size of the LUT depends on the length of the n-bit PA. If n is large then LUT becomes too large, this slows down the speed of the DDS and results in higher power consumption. A technique of phase truncation (PT) is employed to reduce the size of the LUT. Since in this technique part of the phase generated by the PA is truncated that gives rise to spurs in output spectrum

To minimize these spurs, dither is added to the system that reduces the spurs in output spectrum. Since, the DDFS is a digital system clock jitter also introduces noise in the output spectrum. Jitter is an abrupt and unwanted variation of one or more signal characteristics, as the interval between the amplitude of successive cycles, successive pulses, or the frequency or phase of successive cycles.

With advances in design and process technology, today's DDFS devices are very compact and draw little power. The ability to produce and control waveforms accurately various frequencies and profiles has become a key requirement common to a number of industries. Providing agile sources of low-phase-noise variable-frequencies with good spurious performance for communications, or generating a frequency stimulus in industrial or biomedical test equipment applications, compactness, convenience, and low cost are important design considerations. Frequency generation are open to a designer, ranging from phase-locked-loop (PLL)-based techniques for very high-frequency synthesis, dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. The DDFS technique is rapidly gaining acceptance for solving frequency- (or waveform) generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

2. DIRECT DIGITAL FREQUENCY SYNTHESIZER ARCHITECTURE

The main aim of the project is to implement direct digital frequency synthesizer that can implement wave forms like sine wave, square wave, triangular and ramp waveforms. The main blocks in the project are phase accumulator, waveform generator, and selection switches. The first block is the phase accumulator for

which clock, input data to be modulated, and the frequency control word are the inputs. The phase accumulator used is a sixteen bit accumulator. The output will be the phase values. The next block is the waveform generator, for which the output of phase accumulator is given as input. This will generate the amplitude values for the corresponding phase values. The output will be the final modulated waveform. Here we are implementing all digital modulations; the selection of type of modulation is done with the help of selection switches. This selection switches are present on the Basys board. We can do modulation for four different digital data and that data is specified in code. The data selection is also done with selection switches only.

The code for all the above blocks is written in VHDL. All the blocks are functional simulated using ModelSim to verify the functionality of the design .Then the design is synthesized using Xilinx ISE and the design is implemented on to Spartan-3E FPGA by giving Area and timing constraints. In this Basys circuit board is used. The Basys board is a circuit design and implementation platform that anyone can use to gain experience building real digital circuits. This is built around a Xilinx Spartan-3E Field Programmable Gate Array and a Cypress EZUSB controller. Basys board provides complete, hardware suitable for hosting circuits ranging from basic logic devices to complex controllers.

All the generated waveforms are going to be shown using chip-scope tool. The Chip Scope Pro tools integrate key logic analyzer and other test and measurement hardware components with the target design inside Xilinx Virtex™, Spartan-3, and Spartan-3E. The Chip Scope Pro tools communicate with these components and provide the designer with a robust logic analyzer solution. In this project MATLAB is used for generating the amplitude values. Actually the system clock is 50MHz, but from that clock we are generating 13.3 KHz clock which is used as main clock for our design.

2.1 DDS Architecture

The DDS is referred as a Numerically-Controlled Oscillator (NCO), but since no element of the DDS "oscillates" (in fact, this is one of the concept's most important features) that is a misnomer, and of the three classic techniques only the DDS truly "synthesizes" the output waveform, this document will hereafter use "DDS".

The DDS seems architecturally simple, yet provides persuasive advantages that are difficult or expensive to achieve with alternative synthesis methods. Advantages include very fast switching (typically sub microsecond) which is important in frequency-hopping systems or spread-spectrum, including commercial spectroscopy and automatic test equipment (ATE) systems, and system can't change frequencies as rapidly as a DDS. Other advantages include fine steps, excellent phase noise, transient-free (phase continuous) extraordinary flexibility as a modulator, small size, frequency changes, and among others.

There are disadvantages also, of which two impose serious restrictions upon the designer. DDS covers an operating range limited by sampling theory (Shannon, Nyquist). Practically, the output is limited to about 45% of the maximum clock rate at which the logic can be operated. The broadest bandwidth DDS achieved has been clocked over 1GHz, with an output of 450MHz bandwidth. The second limitation is spectral purity, which is density/complexity of the logic circuitry that is attainable at the desired operating speed. Operating bandwidth and Spectral purity are inversely correlated, will be shown. Limitations, the DDS has evolved an important tool, and its functional capabilities are not attainable with any other signal generation technique.

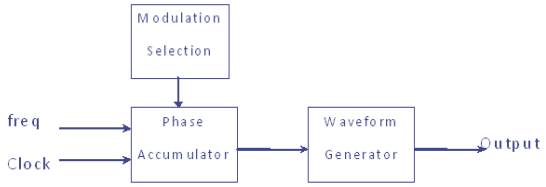


Fig 2.1: Block Diagram of ddfs

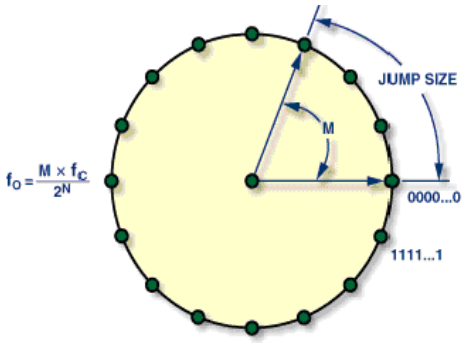
3. PHASE ACCUMULATOR

Phase Accumulator is the most important block in this project. This block is used to accumulate the value of a Frequency Control Word (FCW) at every clock cycle. The value presented at the output of the Phase Accumulator is used as the address for a Read Only Memory, where the samples of a sinusoidal signal are stored. The phase accumulator is actually a modulo-*M* counter that increments its stored number each time it receives a clock pulse.

3.1 Working of Phase Accumulator

Visualize the sine-wave oscillation as a vector rotating around a phase circle. Each point on the phase wheel corresponds to the equivalent point on a cycle of sine wave.

Continuous-time sinusoidal signals have a repetitive angular phase range of 0 to 2π. As the vector rotates around the wheel, the angle generates a corresponding output sine wave. Revolution of the vector around phase wheel, with constant speed, results in one complete cycle of the output sine wave. The accumulator provides the equally spaced angular values accompanying the vector's linear rotation around the phase wheel. The contents of accumulator correspond to the points on the cycle of the output sine wave.



n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

Fig 2.2: Digital phase wheel

The phase accumulator is actually a modulo-*M* counter that increments its stored number each time it receives a clock pulse. Magnitude of the increment is determined by the binary-coded input word (*M*). This word forms the phase step size between

reference-clock updates; it effectively sets how many points to skip around the phase wheel. Larger the jump size, the faster the phase accumulator overflows and completes it's equivalent of a sine-wave cycle. Number of discrete phase points contained in the *wheel* is determined by the resolution of the phase accumulator (*n*).

3.2 DDS Evolution

The most obvious "trade-offs" in a DDS are speed (BW) and spectral purity. The denser the circuitry the more accurately the output waveform will be defined, and better the spurs will be suppressed - but hence BW, limits speed, additional circuitry etc.

Other factors include modulation functions, switching speed or chirp rate (pipelining), etc. As the technology is grown so complex and diverse that there are some DDS capabilities that are mutually exclusive.

Today's DDS products are available at several levels of integration. Its (DDS) capabilities are available as a card for the IBM-PC, an instrument, a complete subsystem on a board, in a module, or in a hybrid, while others are sold only as chips or chip sets, to be integrated, by the user and are added to the system.

3.3 Waveform Generator

The output for the previous block is phase word, which will be the input for this block. Waveform generator is used for generating the carrier wave, which is used for modulation of the digital data.

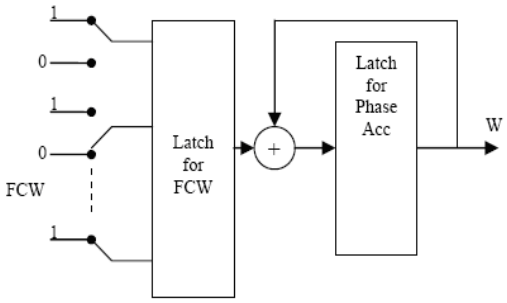


Fig 2.3: phase accumulator

$$f_{OUT} = \frac{M \times f_C}{2^n}$$

f_{OUT} = output frequency of the DDS

M = binary tuning word

f_C = internal reference clock frequency (system clock)

n = length of phase accumulator, in bits

Here we are generating 26 KHz sine waveform. The output of this block is modulated signal, which may be either ASK, FSK, BPSK or QPSK signal.

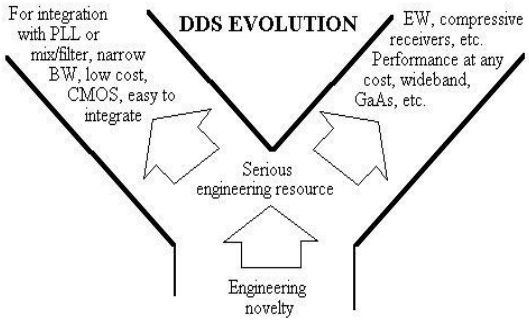


Fig 3.1 DDS Evaluation

3.3.1 Working of Waveform Generator

As we know that for modulating a digital data, first we need a carrier signal. For generating that signal we are using this waveform generator. For this purpose we are using MATLAB

The MATLAB code is as follows

```
p=0:63;

q=sin(2*pi*p/64);

sin_wave1=31*q(1:64);

sin_wave=31*q(1:32);

sin_wave_bin=dec2bin(sin_wave,16);
```

TOP LEVEL DESIGN

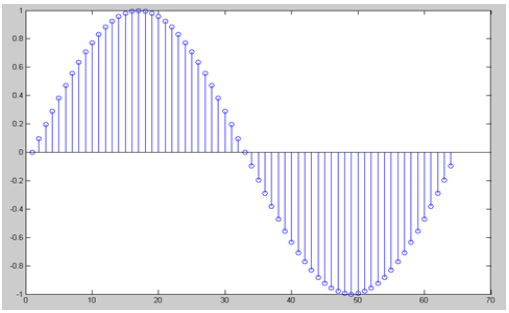


Fig. 3.2 sampled values from MATLAB for waveform generator

4. CONCLUSION

In this project we have been successfully implemented DDFS and simulated using ISE simulator, synthesis by using xilinx9.1i and targeted as Spartan 3e FPGA. In this project we have been successfully generated sine wave, square wave, ramp wave and triangular wave forms. Since this generates sine wave, square wave, ramp wave and triangular wave forms, this allows the user to

Fig 3.3 Block diagram of ddfs

select the frequency according to their wish without changing the equipment as we are doing in general frequency changer.

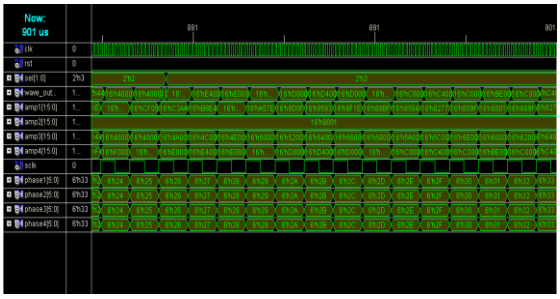


Fig 3.4 simulation results of top level design

PT10VL1602 Project Status			
Project File:	pt10vl1602.ise	**Current State:**	Synthesized
Module Name:	ddfstop	**• Errors:**	No Errors
Target Device:	xc3s250e-4tq144	**• Warnings:**	3 Warnings
Product Version:	ISE 9.1i	**• Updated:**	Fri Sep 7 05:43:40 2012

PT10VL1602 Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	78	2448	
Number of Slice Flip Flops	43	4896	
Number of 4 input LUTs	151	4896	
Number of bonded IOBs	22	108	
Number of BRAMs	4	12	
Number of GCLKs	1	24	

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Sep 7 05:43:39 2012	0	3 Warnings	11 Infos
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					

Fig 3.5 Design summary for top level design

These simulations have provided a better understanding of the response of DDFS with variation of frequencies.

Future Scope

The features of this DDFS are we can generate frequencies of the order GHz and the output will be high amplitude. The system will be optimized to give better spurious free dynamic range.

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