Transformerless Hybrid Power Filter Based On a Six-Switch Two-Leg Inverter for Improved Harmonic Compensation Performance

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Abstract: One of the most important issues is related to current harmonics generated by the increasing number of nonlinear loads connected to the power grid, such as diode and thyristor front-end rectifiers. As a consequence, these harmonics can cause voltage distortions, additional losses in the power system, and malfunction of sensitive electronic equipment. For this reason, harmonic restriction standards, such as IEEE 519, have been recommended to limit the harmonic currents injected into the grid by nonlinear loads. Shunt passive filters, consisting of tuned LC filters and high pass filters, have been traditionally used as a simple and low cost solution to compensate current harmonics. Nevertheless, their performance strongly depends on the grid impedance and can possibly cause the unwanted parallel resonance phenomena with the grid.

Keywords: Active Power Filters (APFs), Diode Rectifiers, Harmonics; Hybrid Power Filters (HPFs).

I. INTRODUCTION

Power quality has become an important issue in recent days. This is due to the huge number of electrical devices of different standards are being connected to the grid. Equipment becomes more advanced, complicated and in fact more sensitive to quality of power supply. On the other hand, a lot of power electronic devices like power switches, UPS systems etc. connects the load to common network and generates distortion (higher harmonics). Earlier problem related to harmonic was marginal but now it has become very serious problem due to the connection of non-linear power electronic devices into the system. Harmonic distortion reduces the life time of the equipment and can interfere with communication lines and sensitive equipment. Conventional harmonic compensation method is installation of passive filters based on LC elements tuned to particular frequency. This method is relatively easy to implement, however, there are few disadvantages as problems with resonance, size and price of passive elements, dependency on temperature and frequency, etc. The drawback of passive filter is overcome by the shunt active filter which consist of voltage source inverter with a large capacitor on its DC link, is considered a well-established solution to reduce the current harmonics to the recommended standard limits.

The major drawback of shunt active power filters is the high-power rating components required to compensate high peak harmonic currents and their associated costs. An alternative to active power filter (APF) is hybrid power filter (HPF), combination of active filters and passive filters. Such a combination with the passive filter makes it possible to significantly reduce the rating of the active filter. The task of the active filter is not to compensate for harmonic currents produced by the thyristor rectifier, but to achieve, harmonic isolation between the supply and the load. As a result, no harmonic resonance occurs. A hybrid filter topology have a common drawback that a large number of passive components and transformer that directly influence the size and weight of these filter. Therefore greater effect has been made to reduce the components in HPFs.

II. EXISTING AND PROPOSED SYSTEMS

A. Existing System

SAPF consists of two basic units: one is three-phase voltage source inverter (VSI) with a capacitor in DC side, the other one is LCL output filter. Total inductance is determined by the capability of APF. Moreover, damping ratio, resonant frequency and attenuation degree of switching ripples are the most crucial factors to design parameters of LCL filters. A method to consider them comprehensively is provided. Meanwhile, LCL filter deteriorates the compensation effect of APF.

B. Proposed System

The SSTL inverter can be seen as two three-phase inverter units connected in series with two passive LC filters tuned in different harmonic frequencies as shown in Fig.1. The top unit, consisting of outputs ABC, is connected to the PCC through LC filters tuned around the seventh harmonic component and is responsible to eliminate the harmonic pair fifth and seventh and also to maintain the dc-link voltage constant in a desired value. Similarly, the bottom unit, represented by the outputs RST, is connected to the PCC through LC filters tuned around the 13th harmonic.
component, being responsible for compensating the harmonic pair 11th and 13th. Thus, the aim of the proposed topology is to obtain a superior compensation capability when compared with conventional HPFs, without increasing the number of switches in the active filter.

Fig.1. Circuit Diagram.

Advantages:
- HPFs are connected to the grid without any matching transformer.
- Improvement in the harmonic compensation performance.

Applications:
- Welding application
- Saw mills

III. HARMONIC INDICES

The power quality industry has developed certain indices values to relate the quality of service with distortion caused by harmonics. The most commonly used indices for measuring harmonic distortion are

A. Total Harmonic Distortion (THD)

A total harmonic distortion is the term used to describe net deviation of waveform from fundamental sin wave. THD is the ratio of RMS value of harmonic to RMS value of fundamental.

$$\text{THD}_h = 100 \sqrt{\frac{U_{h}^2}{U_1^2}}$$  \hspace{1cm} (1)

Where U1 represent fundamental component, Uh represent harmonic component and h represent harmonic order.

B. Total Demand Distortion (TDD)

The TDD index is most often describes current harmonic distortion. Total Demand Distortion is defined as the ratio of square root of the sum of the squares of the RMS value of the currents from 2nd to hth maximum harmonic to peak load demand current.

$$\text{TDD}_{\text{peak demand}} = 100 \sqrt{\frac{I_{\text{rms, distortion}}^2}{I_{\text{peak, max}}}}$$  \hspace{1cm} (2)

Where IRMS distorted is the RMS value of the distorted waveform with the fundamental left out of the summation, and Id max is the peak load demand current at the fundamental frequency.

The utility is responsible for maintaining the quality of the overall system Fig.2. Summarizes the voltage distortion guidelines for different system voltage levels.

Fig.2. IEEE 519-1992 harmonic distortion limit.

IV. EXPERIMENTAL RESULTS

The block diagram of the proposed SSTL HPF prototype is shown in Fig. 3. The quantities measured from the system are the grid currents i_{\text{ABC}}, the load currents i_{\text{LABC}}, the PCC voltages v_{\text{PCCABC}}, and the dc-link voltage v_{\text{dc}}, as shown in Fig. 3. The system parameters are given in Table I.

Fig.3. Experimental setup of proposed transformer less HPF based on the SSTL inverter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid voltage amplitude (line-to-line)</td>
<td>V_S</td>
<td>220V</td>
</tr>
<tr>
<td>Grid frequency</td>
<td>f_S</td>
<td>60Hz</td>
</tr>
<tr>
<td>Switching and sampling frequency</td>
<td>f_{SW}, f_{samp}</td>
<td>20kHz</td>
</tr>
<tr>
<td>De-link voltage reference</td>
<td>v_{dc}</td>
<td>120V</td>
</tr>
<tr>
<td>De-link capacitor of the SSTL inverter</td>
<td>C_{dc}</td>
<td>4700 \mu F</td>
</tr>
<tr>
<td>Top filter capacitor (7th harmonic)</td>
<td>C_{F7H}</td>
<td>30.7 \mu F</td>
</tr>
<tr>
<td>Top filter inductor (7th harmonic)</td>
<td>L_{F7H}</td>
<td>5mH</td>
</tr>
<tr>
<td>Bottom filter capacitor (13th harmonic)</td>
<td>C_{F13H}</td>
<td>61.2 \mu F</td>
</tr>
<tr>
<td>Bottom filter inductor (13th harmonic)</td>
<td>L_{F13H}</td>
<td>0.8mH</td>
</tr>
<tr>
<td>Top filter resonant frequency</td>
<td>f_{F7H}</td>
<td>406.2Hz</td>
</tr>
<tr>
<td>Bottom filter resonant frequency</td>
<td>f_{F13H}</td>
<td>719.3Hz</td>
</tr>
<tr>
<td>Nonlinear load input inductor</td>
<td>L_{I}</td>
<td>1.3mH</td>
</tr>
<tr>
<td>Nonlinear load dc-link resistor</td>
<td>R_{L}</td>
<td>33\Omega</td>
</tr>
</tbody>
</table>

The hardware platform used to control the SSTL inverter is a dSPACE development modular system based on a DS1005 processor board and several boards for each special hardware task, i.e., DS5101 board for PWM generation, DS2004 board for A/D conversion, and DS4002 board for Digital I/O. All
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boards are hosted in a dSpace PX10 expansion box that uses the DS817 board for bidirectional communication with a PC through optical fibers. Due to the nature of the system, some attention should be given during the prototype startup and its insertion in the grid. This insertion operation is performed by switches $S_1$ and $S_2$, as shown in Fig. 3. When switch $S_1$ is closed, both sets of LC filters are charged by the grid through a resistor $R$. After the transient, switch $S_2$ is closed. During the insertion procedure, all top and middle switches ($S_A$, $S_R$, $S_AR$, and $S_S$) of the SSTL inverter must be in on state; and all bottom switches ($S_R$, $S_S$) must be in off state. This is mandatory in order to avoid a premature charging of the dc-link capacitor. A similar procedure for a transformer less HPF based on a conventional VSI was reported.

![Fig.4. Steady-state operation of the HPF based on the SSTL inverter with both top and bottom units off. From top to bottom (10 A/div, 10 ms/div): grid current $i_{Sa}$; load current $i_{La}$; filter current (top unit) $i_{F_{TOP}}$; filter current (bottom unit) $i_{F_{BOT}}$.](image1)

Based on the design guidelines for the LC passive filters described, the values of $L_{TOP}$ and $C_{TOP}$, as shown in Table I, resulted in a resonance frequency of 406.2 Hz, i.e., in the vicinity of seventh harmonic. Similarly, the values of $L_{BOT}$ and $C_{BOT}$ resulted in a resonance frequency of 719.3 Hz, i.e., around the 13th harmonic. Based on these parameters, the dc voltage component that appears in each capacitor of the passive filters was determined using

$$v_{F_A} = -\frac{1}{3}v_{dc}, v_{F_R} = \frac{1}{6}v_{dc}$$
$$v_{F_B} = -\frac{1}{3}v_{dc}, v_{F_S} = \frac{1}{6}v_{dc}$$
$$v_{F_C} = -\frac{2}{3}v_{dc}, v_{F_F} = \frac{1}{3}v_{dc}$$

(2)

Similarly, the output voltages of the SSTL inverter should be able to synthesize the compensating harmonic currents that flow through the passive filters. Nevertheless, depending on the dc-link voltage value, the peaks of the output voltages could not be synthesized, compromising the HPF performance. In order to choose the adequate dc-link voltage value for the proposed HPF, the guideline defined has been followed. For this particular prototype, the dc-link voltage has been set to 120 V. The experimental results of the proposed HPF based on the SSTL inverter are shown in Figs. 4 to 14. The results were obtained through an oscilloscope and a power analyzer to identify the harmonic content in the system. All oscilloscope Figs. 4 to 10 present waveforms for phase $a$ in the following order: grid current $i_S$, load current $i_L$, top filter current $i_{F_{TOP}}$, and bottom filter current $i_{F_{BOT}}$. In order to notice the effect of each inverter unit in the harmonic compensation, the steady-state performance is presented in four different scenarios: only with passive filters; passive filters working with the top inverter unit on; passive filters working with the bottom inverter unit on; and, finally, passive filters with both inverter units working together. The performance of both sets of passive filters, tuned in the seventh and 13th harmonic frequencies, is shown in Fig. 4. The total harmonic distortion (THD) of the load current is about 24% as shown in Fig. 5, which also presents the individual contribution of each harmonic component up to the 13th harmonic. As expected, the performance only with passive filters is poor. The operation of the SSTL top inverter unit with the both sets of passive filters is shown in Fig.6. For this case, the THD for phase $a$ is shown in Fig. 7, which was reduced from 24.8% to 10%.

![Fig.5. Load current distortion indexes.](image2)

![Fig.6. Steady-state of the HPF based on the SSTL inverter with top inverter unit on. From top to bottom (10 A/div, 10 ms/div): grid current $i_{Sa}$; load current $i_{La}$; filter current (top unit) $i_{F_{TOP}}$; Filter current (bottom unit) $i_{F_{BOT}}$.](image3)
The influence of fifth harmonic was strongly reduced from 22.5% to 5.6%, as well as the seventh harmonic, which experienced a reduction from 7.9% to 4.5%. Similarly, it is possible to see the operation of the SSTL bottom inverter unit in Figs. 8 and 9. The 11th and 13th harmonics present indexes of 0.1% and 0.8%, respectively. Comparing with the former results, when the top inverter unit is off, the fifth harmonic component was increased to 7.7%. It is also possible to see that the seventh harmonic component has not been changed. This is due to the presence of a passive filter.

In order to evaluate the effect of background harmonic voltage on the system compensation performance, two different scenarios have been considered. In the first analysis, the nonlinear load has been turned off in order to understand the interaction of the background harmonic voltage with passive filters. Meanwhile, in the second analysis, the nonlinear load is connected to the system to evaluate the compensation performance of the system in the presence of background harmonic voltage. The worst case scenario occurs when seventh and tuned in the vicinity of the seventh harmonic frequency. Finally, the performance of both inverter units is presented in Figs. 10 and 11. The THD of grid current is about 4%, which means the SSTL performance meets the IEEE 519 standard. In addition, it is possible to see that all harmonic components have been reduced when compared with the harmonic table presented in Fig. 6. This effectively proves that SSTL system is working on the compensation of the predominant harmonics from the fifth to 13th. Finally, the transient performance of HPF based on the SSTL inverter with both inverters units on is shown in Fig. 12 for a load step change from 0% to 100%. It is possible to see that the dc-link voltage is almost constant during the step change, meaning that the connection of LC filters in terminals...
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P and N does not bring any stability problem as the connection in terminal o does.

Fig.11. Grid current distortion indexes for both top and bottom inverter operation.

Fig.12. Transient response of HPF based on the SSTL inverter with top and bottom units on. From top to bottom (50 ms/div): Grid current \(i_{sa}\) (10 A/div); Load current \(i_{la}\) (10 A/div); Filter current (top unit) \(i_f\) (top) (10 A/div); Filter current (bottom unit) \(i_f\) (bot) (10 A/div); dc-link voltage \(v_{dc}\) (10 V/div, AC coupling).

Fig.13. Transient response of HPF based on the SSTL inverter when the active filter is enabled with no load connected. From top to bottom (20 ms/div): Grid current \(i_{sa}\) (10 A/div); Load current \(i_{la}\) (10 A/div); Filter current (top unit) \(i_f\) (top) (10 A/div); Filter current (bottom unit) \(i_f\) (bot) (10 A/div).

13th harmonic components are presented in grid voltage, since the passive filters are tuned on those frequencies. Thus, 2.6% of seventh and 3% of 13th harmonic components have been introduced in the grid voltage for both scenarios. The transient response of the proposed system with no load connected is shown in Fig. 13. As expected, there is an interaction of the background harmonic voltage with the passive filters, since they present zero impedance (approximately) for seventh and 13th harmonic components. When the active filter is enabled, the THD of the grid current is reduced from 36% to 3%, showing that the resonance is strongly attenuated. On the other hand, the case where the load is connected to the system is shown in Fig. 14. Once more, when the active filter is enabled, the THD of the grid current is reduced from 43% to 5.6%. This proves the effectiveness of the proposed topology to reduce the effect of the resonance and to compensate the harmonic currents of the load at the same time. It worth mentioning that, since the proposed system is only capable of reducing (not eliminating) the resonance, the performance is slightly compromised. Nevertheless, two remarks should be pointed out: it is considered a highly distorted grid, with a 4% of voltage THD (in general, the voltage distortion is much lower than 4%); it is always possible to increase the values of \(k_{top}\) and \(k_{bottom}\), reducing even more the resonance and the THD of the grid current. As consequence, a higher dc-link voltage is needed in order to avoid the saturation of the PWM duty cycles. Therefore, a compromise between system performance and dc-link voltage value should be evaluated.

V. CONCLUSION

This paper explains about transformerless HPF topology on six switch inverter. The proposed system consists of two three phase inverter connected in series with the two passive LC filters tuned to desired frequency and the number
of switches are reduced when compared to other dual topology, aiming an improvement in the harmonic compensation performance. The results obtained from simulation of system using MATLAB program show that the proposed controller effectively cancels the harmonic components of the source current.

VI. REFERENCES


