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Upgrading Power Quality of Power Generated by Renewable Energy Sources by using Voltage Restrained D-STATCOM

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Abstract: This paper suggests us a new design to develop reference voltage for a distribution static compensator (D-STATCOM) which works in voltage-control mode. The new design has more gains related to old voltage-control D-STATCOM where reference voltage is promptly taken as 1.0 p.u. The new design assures that UPF is attained at load terminal during nominal operation, which is not achievable in old design. Moreover, a retaining in rating of D-STATCOM is attained that boosts its scope to mitigate voltage sag. Virtually UPF is managed, although improving voltage at the load terminal, all along load change. This design grant DSTATCOM to hook PQ problems by lending pf improvement, harmonic destruction, load adjusting and voltage control positioned on load demand.

Keywords: Current Control Mode, Power Quality(PQ), Voltage-Control Mode, Voltage-Source Inverter.

I. INTRODUCTION

A Distribution system suffers from current as well as voltage-related power-quality (PQ) problems, which include poor power factor, distorted source current, and voltage disturbances [1], [2]. A DSTATCOM, connected at the point of common coupling (PCC), has been utilized to mitigate both types of PQ problems [2]–[12]. When operating in current control mode (CCM), it injects reactive and harmonic components of load currents to make source currents balanced, sinusoidal, and in phase with the PCC voltages [3]–[7]. In voltage-control mode (VCM) [2], [8]–[12], the DSTATCOM regulates PCC voltage at a reference value to protect critical loads from voltage disturbances, such as sag, swell, and unbalances. However, the advantages of CCM and VCM cannot be achieved simultaneously with one active filter device, since two modes are independent of each other.

In CCM operation, the DSTATCOM cannot compensate for voltage disturbances. Hence, CCM operation of DSTATCOM is not useful under voltage disturbances, which is a major disadvantage of this mode of operation [13]. Traditionally, in VCM operation, the DSTATCOM regulates the PCC voltage at 1.0 p.u. [2], [8]–[11]. However, a load works satisfactorily for a permissible voltage range [14]. Hence, it is not necessary to regulate the PCC voltage at 1.0 p.u. While maintaining 1.0-p.u. voltage, DSTATCOM compensates for the voltage drop in feeder. For this, the compensator has to supply additional reactive currents which increases the source currents. This increases losses in the voltage-source inverter (VSI) and feeder. Another important aspect is the rating of the VSI. Due to increased current injection, the VSI is de-rated in steady-state condition. Consequently, its capability to mitigate deep voltage sag decreases. This paper considers the operation of DSTATCOM in VCM and proposes a control algorithm to obtain the reference load terminal voltage. This algorithm provides the combined advantages of CCM and VCM. The UPF operation at the PCC is achieved at nominal load, whereas fast voltage regulation is provided during voltage disturbances. The discrete PWM controller is used to generate switching pulses. The control strategy is tested with a three-phase four-wire distribution system. The effectiveness of the proposed algorithm is validated through detailed simulation and experimental results.

II. PROPOSED CONTROL SCHEME

Circuit diagram of a DSTATCOM-compensated distribution system is shown in Fig. 1. It uses a fuel cell, universal bridge of three-level, neutral-point-clamped VSI. This structure allows independent control to each leg of the VSI [7]. Fig. 2 shows the single-phase equivalent representation of Fig1. Filter inductance and resistance are Lf and Rf, respectively. Shunt capacitor Cfc eliminates high-switching frequency components.

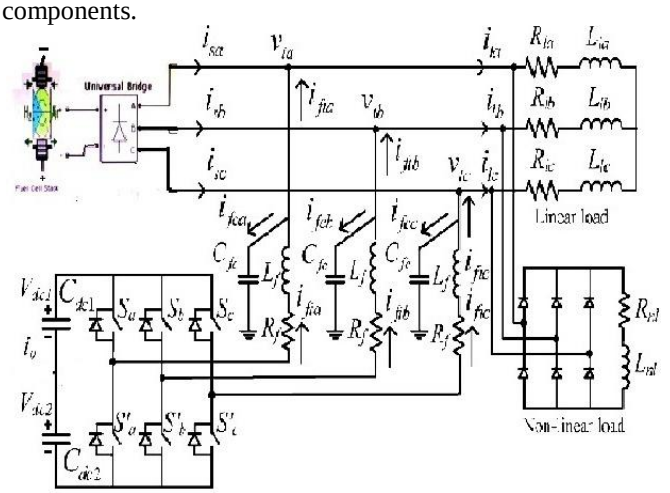

Fig.1. Circuit diagram of DSTATCOM-compensated distribution system.

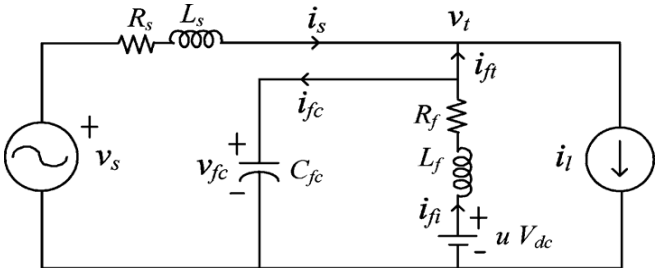

Fig. 2. Single-phase equivalent circuit of DSTATCOM.

It is shown that the PCC voltage can be regulated to the desired value with properly chosen parameters of the VSI. Then, a procedure to design VSI parameters is presented.

III. DESIGN OF VSI PARAMETERS

DSTATCOM regulates terminal voltage satisfactorily, depending upon the properly chosen VSI parameters. The design procedure of these parameters is presented as follows.

1. Voltage Across DC Bus (Vdc): The dc bus voltage is taken twice the peak of the phase voltage of the source for satisfactory performance [19]. Therefore, for a line voltage of 400 V, the dc bus voltage is maintained at 650 V.

2. DC Capacitance (Cdc): Values of dc capacitors are chosen based on a period of sag/swell and change in dc bus voltage during transients.

$$C_{\rm dc} = \frac{2\,p\,S\,T}{V_{\rm dcref}^2 - V_{\rm dc}^2}. \tag{1}$$

Here, S=10 kVA, Vdcref=650 V, p=1, and Vdc= 0.8 Vdcref or 1.2 Vdcref. Using (1), capacitor values are found to be 2630 uf and 2152 uf. The capacitor value 2600 uf is chosen to achieve satisfactory performance during all operating conditions.

3. Filter Inductance (Lf): Filter inductance (Lf)should provide reasonably high switching frequency and a sufficient rate of change of current such that VSI currents follow desired currents.

$$L_f = \frac{2\,V_m}{(2\,h_c)\,(2\,f_{\rm max})} = \frac{0.5\,V_m}{h_c\,f_{\rm max}} \tag{2}$$

Where 2hc is the ripple in the current. With fmax=10 kHz and hc=0.75 A (5% of rated current), the value of Lf using (2) is found to be 21.8 mH, and 22 mH is used in realizing the filter.

4. Shunt Capacitor(Cfc): The shunt capacitor should not resonate with feeder inductance at the fundamental frequency(wo). Capacitance, at which resonance will occur, is given as

$$C_{fcr} = \frac{1}{\omega_o^2\,L_s}. \tag{3}$$

For proper operation, Cfc must be chosen very small compared to Cfcr (3). Here, a value of 5 uF is chosen which provides an Z=637ohm at wo. This does not allow the capacitor to draw significant fundamental reactive current.

In the traditional method, the reference voltage is 1.0 p.u. [2], [8]– [11], whereas in the proposed method, equation (4) is used to find the reference voltage.

$$V_t^* = \sqrt{V^2 - \left(\left|\bar{I}_{la1}^{+}\right| X_s\right)^2} - \left|\bar{I}_{la1}^{+}\right| R_s. \tag{4}$$

TABLE I
SIMULATION PARAMETERS

System quantities	Values
Source voltage	400 V rms line to line, 50 Hz
Feeder impedance	$Z_s = 1 + j3.14\ \Omega$
Linear load	$Z_{la} = 30 + j62.8\ \Omega$, $Z_{lb} = 40 + j78.5\ \Omega$, $Z_{lc} = 50 + j50.24\ \Omega$
Non-linear load	An R-L load of $50 + j62.8\ \Omega$
VSI parameters	$V_{dc} = 650$ V, $C_{dc} = 2600\ \mu$F, $R_f = 1\ \Omega$, $L_f = 22$ mH, $C_{fc} = 5\ \mu$F, $I_{rated} = 30$ A
PI gains	$K_{p\delta} = 8.5\,e^{-7}$, $K_{i\delta} = 1.8\,e^{-6}$
Hysteresis band (h)	1 V

IV. SIMULATION RESULTS

The control scheme is implemented using PSCAD software. Simulation parameters are given in Table I. Terminal voltages and source currents before compensation are plotted in Fig. 3. Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Three conditions, namely, nominal operation, operation during sag, and operation during load change are compared between the traditional and proposed method.

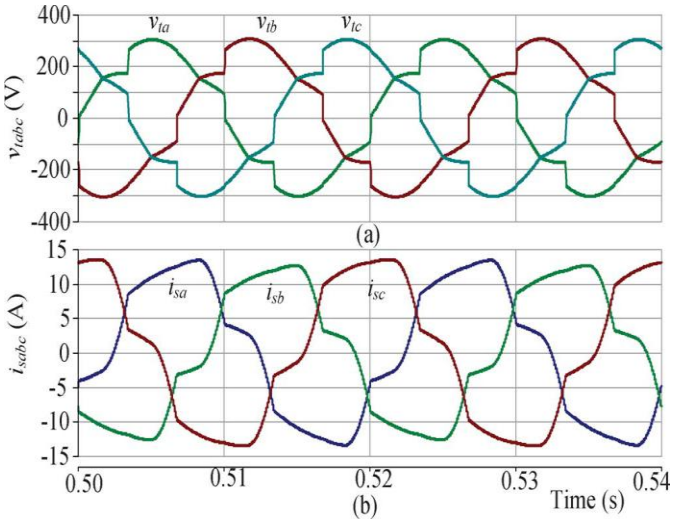

Fig. 3. Before compensation. (a) Terminal voltages. (b) Source currents.

A. Nominal Operation

Initially, the traditional method is considered. Fig. 4(a)–(c) shows the regulated terminal voltages and corresponding source currents in phases a, b and c respectively. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents.

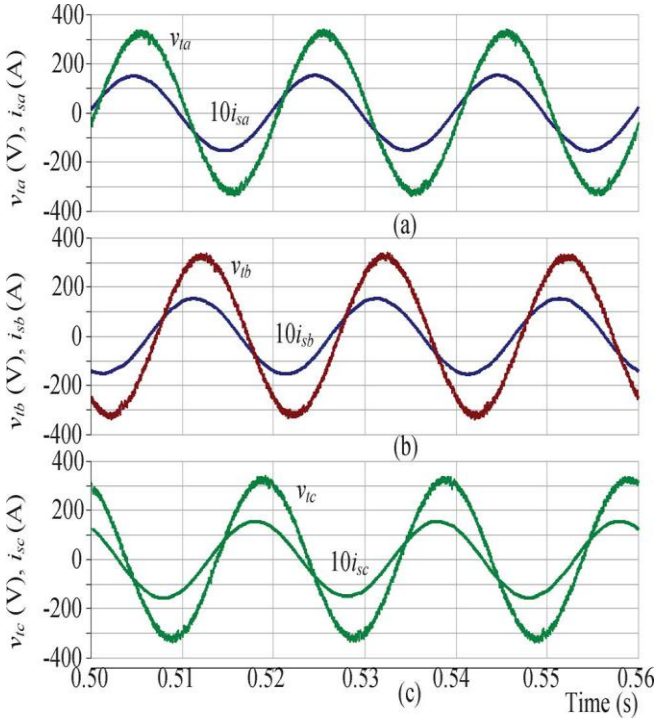

Fig. 4. Terminal voltages and source currents using the traditional method. (a) Phase-a. (b) Phase-b. (c) Phase-c.

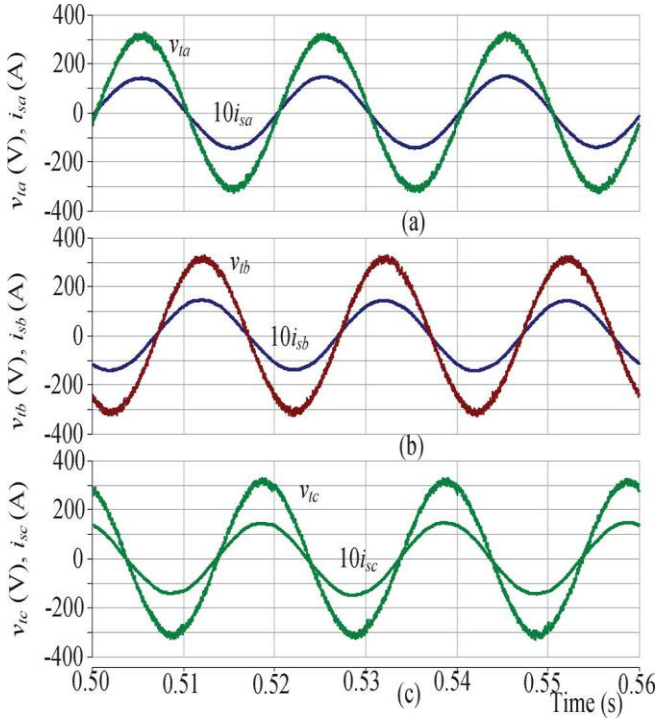

Fig. 7. Terminal voltages and source currents using the proposed method. (a) Phase-a. (b) Phase-b. (c) Phase-c.

Fig. 5(a) shows the dc bus voltage regulated at a nominal voltage of 1300V.Fig5(b) shows the load angle settled around 8.50degrees.

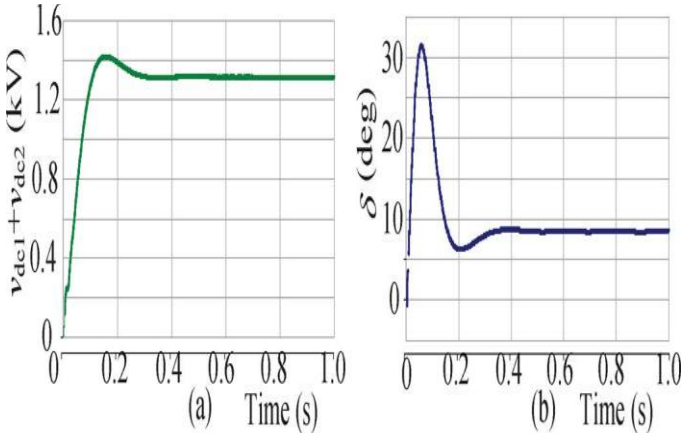

Fig. 5. (a) Voltage at the dc bus. (b) Load angle.

Using the proposed method, terminal voltages and source currents in phases a, b and c are shown in Fig. 6(a)–(c), respectively. It can be seen that the respective terminal voltages and source currents are in phase with each other, in addition to being balanced and sinusoidal. Therefore, UPF is achieved at the load terminal. For the considered system, waveforms of load reactive power (Qload), compensator reactive power (Qvsi), and reactive power at the PCC (Qpcc) in the traditional and proposed methods are given in Fig. 7(a) and (b), respectively. In the traditional method, the compensator needs to overcome voltage drop across the feeder by supplying reactive power into the source.

As shown in Fig. 7(a), reactive power is supplied by the compensator, this confirms that significant reactive current flows along the feeder in the traditional method. However, in the proposed method, UPF is achieved at the PCC by maintaining suitable voltage magnitude. Thus, the reactive power supplied by the compensator is the same as that of the load reactive power demand. Consequently, reactive power exchanged by the source at the PCC is zero. These waveforms are given in Fig. 7(b).

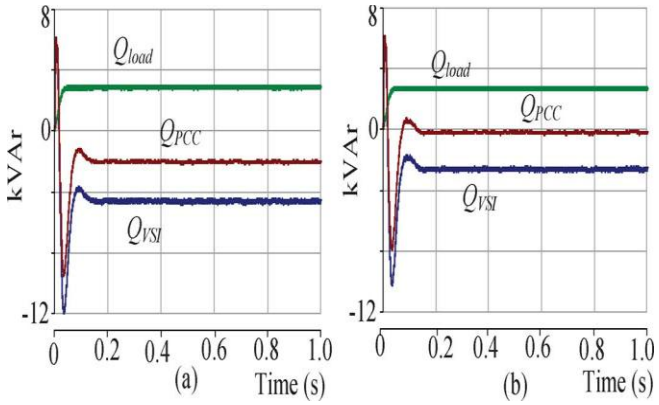

Fig. 7. Load reactive power (Qload), compensator reactive power (Qvsi), and reactive power at PCC (Qpcc). (a) Traditional method. (b) Proposed method.

Fig. 8(a) and (b) shows the source rms currents in phase-a for the traditional and proposed methods, respectively. Consequently, it reduces the ohmic losses in the feeder. Fig. 9(a) and (b) shows the compensator rms currents in phase-afor the traditional and proposed methods, respectively.

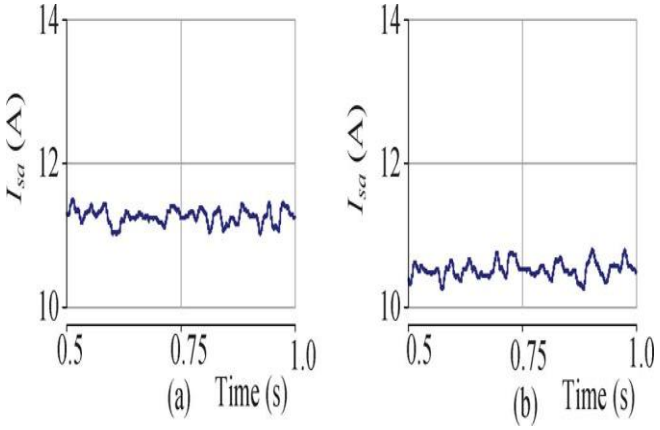

Fig.8. Phase- source rms currents. (a) Traditional method. (b) Proposed method.

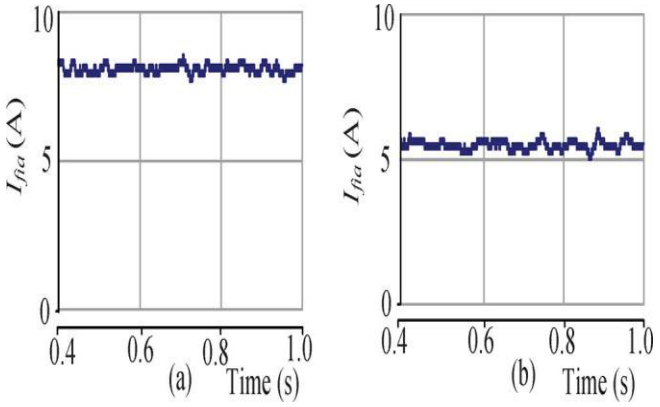

Fig. 9. Phase- compensator rms currents. (a) Traditional method. (b) Proposed method.

VSI losses are reduced by 61.68% and only 61.9% VSI rating is utilized in the proposed method. In the traditional method, DSTATCOM maintains a load terminal voltage at 1.0 p.u. For this, it needs to compensate for the entire feeder drop. However, in the proposed scheme, the compensator does not compensate for the feeder drop in the steady-state condition. Hence, a lesser rating of VSI is utilized in the steady state. This savings in rating is utilized to mitigate deep sag, and D-STATCOM capacity to mitigate deep sag increases.

B. Operation During Sag

To create sag, source voltage is lowered by 20% from its nominal value at t=0.6sec as shown in Fig. 10(a). Sag is removed at t=1.0sec as shown in Fig. 10(b). Fig. 10(c) and (d) shows terminal voltages regulated at their reference value. The controller provides a fast voltage regulation at the load terminal. Fig. 10(e) and (f) shows the total dc bus voltage and the load angle, respectively. During transient period, capacitors supply real power to maintain load power which results in discharging of capacitors. After some time, the dc bus voltage again reaches the reference voltage whereas the load angle settles down at 17.4deg. However, the load angle again settles down at nominal value once sag gets cleared. Compensator rms currents in traditional and proposed method in phase-a are shown in Fig. 10(g) and (h), respectively.

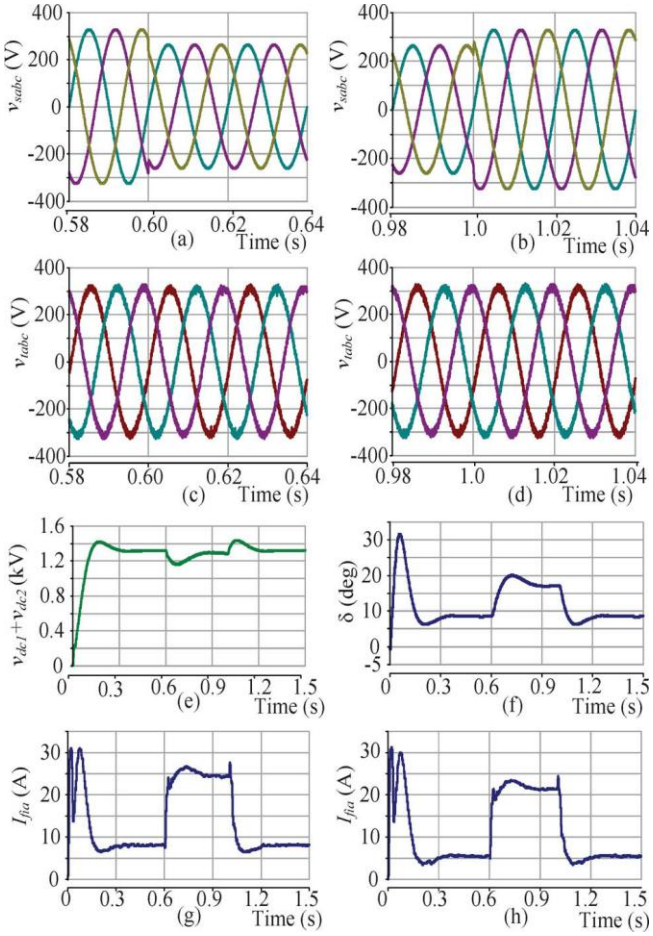

Fig. 11. (a) Source voltages during normal to sag. (b) Source voltages during sag to normal. (c) Terminal voltages during normal to sag. (d) Terminal voltages during sag to normal. (e) Voltage at the dc bus. (f) Load angle. (g) Compensator rms current in the traditional method. (h) Compensator rms current in the proposed method.

Loss reduction in VSI = 484 W
Percentage loss reduction in the VSI = -26.23%.
Savings in utilization of the VSI rating will be 2790 VA.

If the rating of VSI is limited to mitigate 20% sag, then this savings in rating can be used to mitigate additional sag. These waveforms confirm that the DSTATCOM has the capability to mitigate deep sag independent of duration. However, it requires a high current rating of the VSI.

C. Operation During Load Change

To show the impact of load changes on system performance, load is increased to 140% of its nominal value. Under this condition, the traditional method gives less power factor as the compensator will supply more reactive current to maintain the reference voltage. The voltage and current waveforms, as shown in Fig. 12(a), confirm this. In proposed method, a load change will result in small deviation in terminal voltage from its reference voltage. Compensator just needs to supply extra reactive current to overcome this small extra feeder drop,

hence, nearly UPF is maintained while regulating the terminal voltage at its reference voltage. It is evident from Fig. 12(b).

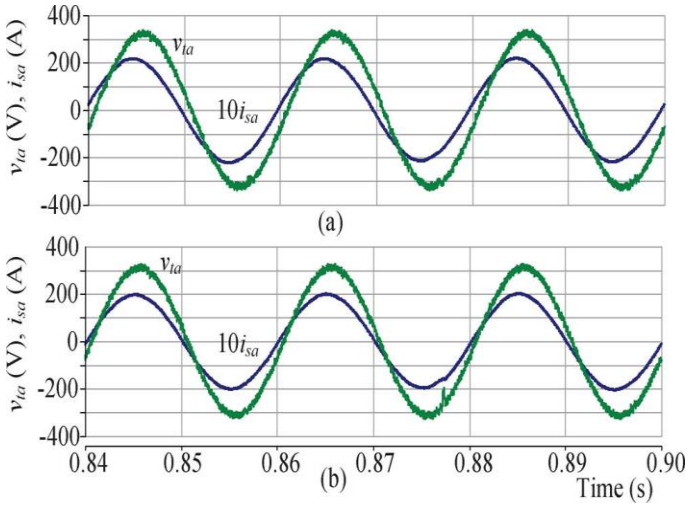

Fig.13. Terminal voltage and source current in phase- during load change. (a) Traditional method. (b) Proposed method.

V. CONCLUSION

In this paper, a new design has been proposed for the generation of reference load voltage for a voltage-restrained DSTATCOM. The performance of the proposed scheme is compared with the traditional voltage-restrained DSTATCOM. The proposed method provides the following advantages: 1) at nominal load, the compensator injects reactive and harmonic components of load currents, resulting in UPF; 2) nearly UPF is maintained for a load change; 3) fast voltage regulation has been achieved during voltage disturbances; and 4) losses in the VSI and feeder are reduced considerably, and have higher sag supporting capability with the same VSI rating compared to the traditional scheme. The simulation results show that the proposed scheme provides DSTATCOM, a capability to improve several PQ problems (related to voltage and current).

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