Modeling and Design of Series Voltage Compensator for Reduced Capacitance in Grid-Tie Solar Inverter with Fuzzy Logic Controller

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Abstract: In this project Design of Series Voltage Compensator for Reduction of DC-Link Capacitance in Grid-Tie Solar Inverter is proposed. A grid-tie solar inverter with a series voltage compensator for reducing the high-voltage dc-link capacitance is presented with both PI and Fuzzy logic controllers. The compensator obtains energy from the dc link to sustain the voltage on its dc side and generates an ac voltage to counteract the voltage ripple on the dc link. As the compensator processes small ripple voltage on the dc link and reactive power, it can be implemented with low-voltage devices, and thus, its volt amp rating is small. As the required energy storage of the dc link, formed by a reduced value of the dc-link capacitor and the compensator, is reduced, the architecture allows replacing popularly used electrolytic capacitors with alternatives of longer lifetime, such as power film capacitors, or extending the system lifetime even if there is a significant reduction in the capacitance of electrolytic capacitors due to aging. Detailed mathematical analysis on the static and dynamic behaviors of the overall system, and the control method will be presented. The simulation results are presented by using Matlab/Simulink system.

Keywords: Capacitors, Capacitor-Supported Systems, DC–AC Power Conversion, Grid-Tie Solar Inverters, Photovoltaic Systems, Reliability, Fuzzy Logic System.

I. INTRODUCTION

A capacitor-supported system consists of multiple power converters interconnected by a dc link. The dc-link voltage is maintained by a capacitor bank that absorbs instantaneous power difference between the input source and output load, minimizing voltage variation on the dc link, and providing sufficient energy during the hold-up time of the system. Among different types of capacitor, aluminum electrolytic capacitors (E-Caps) are the most popular choice because of their high volumetric efficiency and low cost. However, they suffer from the drawbacks of high equivalent series resistance (ESR); low ripple current capability; bottleneck of the voltage rating; relatively short lifetime compared to other components; and considerable maintenance work. Advances in power film capacitor technology are emerging for dc-link filtering [1], [2]. Power film capacitors outperform aluminum E-Caps in terms of ESR, self-healing capability, life expectancy, environmental performance, dc-blocking capability, ripple current capability, and reliability. Although low-voltage and high-value film capacitors are available, the capacitance of the high-voltage film capacitors still cannot complete with E-Caps, due to their relatively low volumetric efficiency and high cost. To lessen the dependency of the dc-link capacitance, there are many prior-art methods, based on the following approaches:

1. Performance trade-off: This method allows a larger voltage ripple across the dc link with a smaller capacitance. However, it is practically less impressive as the system performance will be degraded. It is more suitable for certain applications, like the ones in [3]–[5]. A set of design procedure is given in [6] for the optimization of capacitor bank.

2. Reduction of the dc-link capacitor current with sophisticated control: The concept is based on reducing the ripple current flowing through the dc-link capacitor [7]. The front-stage converter is an active rectifier, and a step-up dc–dc converter in [8], while the output is an inverter. Their key advantage is that no additional circuit is needed. However, those control methods cannot be applied to systems with front-end diode-bridge rectifier. Apart from requiring a sophisticated controller, some of them also rely on specific relationship in the operating frequency between the converters connected [9]. The method given is limited to three-phase systems. The controller described is based on assuming an ideal energy conversion. Thus, the actual input current would be distorted unless multiple cell load inverters are used. The performance of those controllers is greatly dependent on the accuracy of the computations [10] and affected by the overall time delays of the control loops.

3. Increase in the frequency of the dc-link voltage ripple: A double frequency front-end converter with multiphase switching is proposed in [11] to reduce the ripple voltage. However, the approach cannot reduce the dc-link capacitance significantly.

4. Ripple cancellation circuit with a coupled element: In [12], a coupled inductor is applied to cancel the voltage ripple of the dc input, dc output, or dc link of a power

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II. OPERATION OF THE SERIES VOLTAGE COMPENSATOR

Fig 1 shows the architecture of the grid-tie solar inverter system with a series voltage compensator connected to the dc-link. The system consists of two power conversion stages. The front stage is a dc–dc boost converter. It is connected between a string of solar panels and the dc link. The output stage is a grid-tie dc–ac converter, which is connected between the dc-link and the power grid. The compensator, which is a capacitor supported full-bridge dc–ac converter without an external dc source, is connected between the two converters. The voltage compensator generates an ac voltage that counteracts the ripple voltage on the output of the boost converter. Thus, the input of the grid-tie inverter is a dc voltage equal to the average value of the voltage vdc across the dc-link capacitor Cdc. The dc-link voltage vdc and the input voltage of the voltage compensator va are sensed. The scaling factor α is the ratio between Vtric and Va,ref , where Vtric is the amplitude of the triangular carrier signal vtric in the PWM controller and Va,ref is the voltage reference for the input voltage of the voltage compensator. The difference between Va,ref and va is processed by a PI controller G(s) to give an offset voltage vos. The control signal vcon is obtained by combining α vdc with vos. The dc component of α vdc is ideally cancelled in vcon by vos as vos = −αVdc, where Vos and Vd care the dc component of vos and vdc, respectively. With such arrangement, it is unnecessary to use a high-pass filter to extract the ac component of vdc. At the same time, the stable dc level of va can be obtained by Voltage control, which ensures the compensator only handles the reactive power in the steady state. During the steady-state operation, vcon equals the conditioned ac component of avdc. It is then used to compare with the triangular carrier waveform in the pulse width modulation modulator to generate the voltage vab having the same phase and amplitude with ∆vdc.

Without any external power supply, the power dissipation of the voltage compensator is obtained from the dc link. Practically speaking, instead of a pure ac voltage, both vab and vcon consists of not only ac component, but also small amount of the dc component. Since the input current of the grid-tie inverter consists of the dc component, some power will be absorbed by the compensator ifvab consists of the dc component. Derivations of the parameter sin the control.

III. SYSTEM CHARACTERISTICS

The grid voltage vg and the output grid current ig can be expressed as

\[ v_g(t) = V_g \sin \omega t \]  
\[ i_g(t) = I_g \sin(\omega t + \phi) \]

Where Vg and Ig are the amplitude of vg and ig , respectively. ω = 2πf is the angular line frequency, f is the line frequency, and ϕ is the phase difference between vg and ig .Based on (1) and (2), the instantaneous output power pg is

\[ p_g(t) = v_g(t) i_g(t) \]
\[ = \frac{2P_g}{\cos \phi} \sin \omega t \sin(\omega t + \phi) \]

Where Pg =VgIg/2 cos ϕ is the average output power. By applying the Kirchhoff’s current law at the node of the Dc-link capacitor Cdc, the relationship among the output current...
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of the boost converter, the dc-link capacitor current \(i_C\), and input current \(i_d\) of the inverter can be expressed as

\[i_C(t) = i_a(t) - i_d(t)\] (4)

The dominant component of \(\Delta v_{dc}\) is the double of the line frequency harmonics. For the sake of simplicity in the analysis, \(\Delta v_{dc}\) is expressed as

\[\Delta v_{dc}(t) = |\Delta V_{dc}| \sin(2\omega t + \theta)\] (5)

Where \(|\Delta V_{dc}|\) is the magnitude of \(\Delta v_{dc}\) and \(\theta\) is the phase angle of \(\Delta v_{dc}\).

A. Steady-State Characteristics of the Voltage Compensator

Since the voltage compensator counteracts the ripple voltage on the dc-link capacitor only, the input voltage of the grid-tied dc–ac converter, \(v_d\), is equal to \(V_{dc}\). By using (3), the input current of the dc–ac converter, \(i_d\), can be expressed as

\[i_d(t) = \frac{P_g(t)}{V_{dc}} = \frac{P_g}{V_{dc} \cos \phi} \left[\cos \phi - \cos(2\omega t + \phi)\right]\] (6)

By substituting (5) and (6) into (4),

\[\gamma \cos(2\omega t + \theta - \delta) = \frac{P_g}{\lambda V_{dc} \cos \phi} \cos(2\omega t + \phi)\] (7)

Where

\[\gamma = \sqrt{\left(\frac{P_g}{V_{dc}}\right)^2 + (2\omega C_{dc} V_{dc})^2}, \quad \delta = \tan^{-1}\left(\frac{P_g}{2\omega C_{dc} V_{dc}}\right)\]

and \(\lambda = |\Delta V_{dc}| / V_{dc}\) is the ripple factor.

Detailed proof of (7) is given in the Appendix. By equating the magnitude and phase angle of the LHS and RHS of (7), the following equations can be concluded

\[|\Delta V_{dc}| = \frac{P_g}{\gamma \cos \phi}\]

\[\theta = \phi + \delta.\] (8)

By substituting (8) into (5), the ripple voltage on the dc-link capacitor is

\[\Delta v_{dc}(t) = \frac{P_g}{\gamma V_{dc} \cos \phi} \sin(2\omega t + \phi + \delta) = \lambda V_{dc} \sin(2\omega t + \phi + \delta).\] (9)

According to (9), the relationship among the dc-link capacitance \(C_{dc}\), output phase angle \(\phi\), and the ripple factor \(\lambda\) is

\[C_{dc} = \frac{S_g}{2\omega V_{dc}^2} \frac{1}{\lambda^2 - \cos^2 \phi}\] (10)

Where \(S_g\) is the apparent power of the solar inverter. Detailed proof of (10) is given in the Appendix.

Thus, for a given apparent power \(S_g\), the required value of \(C_{dc}\) will increase as the power factor \(\cos \phi\) decreases. Thus, one of the design constraints is based on considering the minimum power factor. For example, as stated in the statutory requirement VDE-AR-N 4105, the minimum power factor is 0.9. As the compensator handles ripple voltage only (i.e., \(v_{ab} = \Delta v_{dc}\)), the ratio between the apparent power handled by the compensator, \(S_{ab}\), and the apparent power of the whole system is

\[
\frac{S_{ab}}{S_g} = \frac{v_{ab,\text{rms}} i_{d,\text{rms}}}{v_{d,\text{rms}} i_{d,\text{rms}}} = \frac{|\Delta V_{dc}|}{2V_{dc}}\] (11)

Where \(v_{ab,\text{rms}}\) and \(i_{d,\text{rms}}\) are the rms values of \(v_{ab}\) and \(i_d\), respectively, and \(v_{d,\text{rms}}\) is the rms value of the input current of the dc–ac converter. Thus, as \(\Delta V_{dc} / V_{dc}\), the power rating of the compensator is much smaller than that of the whole system. The voltage across the capacitor \(C_a\), \(v_a\), is regulated at \(V_{a,\text{ref}}\) by using the control mechanism depicted in Fig. 1. If \(v_a < V_{a,\text{ref}}\), energy will be absorbed from the dc link, and vice versa. When \(v_a = V_{a,\text{ref}}\), the voltage compensator will ideally absorb zero power. Based on (6) and (9), the average power absorbed by the voltage compensator \(P_{ab}\) is

\[
P_{ab} = \frac{1}{T} \int_0^T v_{ab}(t) i_d(t) dt = \frac{P_g^2}{2\gamma V_{dc} \cos^2 \phi}\] (12)

Where the period \(T = \pi / \omega\).

Thus, based on (12), if the compensator only generates the ripple voltage on the dc-link capacitor, it will generate active power. In order to maintain the power balance for stabilizing \(v_a\) at \(V_{a,\text{ref}}\), a small voltage offset at \(v_{ab}\), \(V_{ab}\), appears

\[
V_{ab} = -\frac{P_{ab}}{I_d} = \frac{P_g}{2\gamma \sin \delta}\] (13)

The relationship between \(v_{ab}\) and \(v_a\) can be expressed as

\[
v_{ab}(t) = \frac{v_{\text{cos}}(t)}{V_{\text{tric}}} v_a(t) = \frac{\alpha v_{dc}(t) + v_{\text{cos}}(t)}{V_{\text{tric}}} v_a(t) = \frac{\alpha P_g}{V_{\text{tric}} \cos \phi} \sin(2\omega t + \phi + \delta) v_a(t) + \frac{\alpha V_{dc} + v_{\text{cos}}(t)}{V_{\text{tric}}} v_a(t).
\] (14)

The first term \(\alpha P_g \sin(2\omega t + \phi + \delta) V_{\text{tric}} \cos \phi\) \(v_a(t)\) represents the ripple voltage compensation on the dc-link capacitor. The second term \(\alpha V_{dc} + v_{\text{cos}}(t) / V_{\text{tric}}\) represents the dc component, related to the power balance described in (13). Thus, asymmetrical PWM switching occurs. Fig. 2(a) and (b) present the operating modes of the compensator using a full bridge. When \(S2\) and \(S3\) are on, the capacitor \(C_a\) charged by the load current \(i_d\). Conversely, when \(S1\) and \(S4\) are on, the capacitor \(C_a\) is discharged by \(i_d\). Fig. 2(c) shows the waveforms of the dc-link capacitor voltage \(v_{dc}\), modulating signal \(v_{\text{sig}}\), triangular carrier signal \(v_{\text{tric}}\), and the voltage at \(C_a\).

The dc component on \(v_{ab}\) is very small. It is observed to be 2.1 V, about 0.5% of the average dc-link voltage of 400 V in the 2-kW inverter system, which will be
described. Thus, such dc component is neglected in the following discussion.

Fig 2. Ripple voltage on the input capacitor Ca in the compensator. (a) Operation when S2 and S3 are on. (b) Operation when S1 and S4 are on. (c) SPWM and the ripple voltage generated across Ca.

During the time interval between the time instants t0 and t1 in Fig. 2(c), Ca is charged by the load current. By using (6) and (9)

\[
v(t) = \frac{1}{C_a} \int_{t_0}^{t_1} \left[ i_d(t) - i_C(t) \right] dt
\]

Where \( v_{a, min} \) is the minimum voltage of \( v_a \).

IV. INTRODUCTION TO FUZZY LOGIC CONTROLLER

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometimes even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to dc-to-dc converter system. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of dc-to-dc converter and performance of proposed controllers. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of dc-to-dc converters. The basic scheme of a fuzzy logic controller is shown in Fig 3 and consists of four principal components such as: a fuzzification interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10]. The fuzzy control systems are based on expert knowledge that converts the human linguistic concepts into an automatic control strategy without any complicated mathematical model [10]. Simulation is performed in buck converter to verify the proposed fuzzy logic controllers.

A. Fuzzy Logic Membership Functions:

The dc-dc converter is a nonlinear function of the duty cycle because of the small signal model and its control method was applied to the control of boost converters. Fuzzy controllers do not require an exact mathematical model. Instead, they are designed based on general knowledge of the plant. Fuzzy controllers are designed to adapt to varying operating points. Fuzzy Logic Controller is designed to control the output of boost dc-dc converter using Mamdani style fuzzy inference system. Two input variables, error (e) and change of error (de) are used in this fuzzy logic system. The single output variable (u) is duty cycle of PWM output.
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B. Fuzzy Logic Rules:
The objective of this dissertation is to control the output voltage of the boost converter. The error and change of error of the output voltage will be the inputs of fuzzy logic controller. These 2 inputs are divided into five groups; NB: Negative Big, NS: Negative Small, ZO: Zero Area, PS: Positive small and PB: Positive Big and its parameter [10]. These fuzzy control rules for error and change of error can be referred in the table that is shown in Table I as per below:

Table I. Table rules for error and change of error

<table>
<thead>
<tr>
<th>(e)</th>
<th>NB</th>
<th>NS</th>
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V. MATLAB/SIMULATION RESULTS

Fig 6. Shows the Matlab/Simulink model of proposed converter connected to grid.

Fig 7. Shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under rated condition.

Fig 8. Shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 50% of rated condition.

Fig 9. Shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 10% of rated condition.

Fig 10. Shows the transient response of the system boost voltage Vdc, PV voltage Vpv from full load to 10% load condition.
Fig 11. Shows the transient response of the system boost voltage Vdc, PV voltage Vpv from 10% load to full load condition.

Fig 12. Shows the Matlab/Simulink model of proposed converter connected to grid with series voltage compensator.

Fig 13. Shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under rated condition.

Fig 14. Shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 50% of rated condition.

Fig 15. Shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 10% of rated condition.

Fig 16. Shows the transient response of the system boost voltage Vdc, PV voltage Vpv from full load to 10% load condition.
VI. CONCLUSION

This paper extends the study of the concept proposed, in which a series voltage compensator is used to reduce the dc-link capacitance. Such concept is applied to a grid-tie solar inverter. The modeling and design of the series voltage compensator has been presented. An active series voltage compensator for reducing the dc-link capacitance in a capacitor-supported power electronic system has been proposed. The implementation requires low-voltage devices only, as the dc-link module only handles ripple voltage in the dc-link and reactive power flow in the dc link. The design guidelines for the dc-link module for applications with and without the hold-up time requirement have been described. From the proposed concept is with both controllers we observed that grid current is having less distortions when operated with fuzzy logic controllers than conventional methods.

VII. REFERENCES


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