Improved Double Line Voltages Synthesis Strategies of Matrix Converter for Input/Output Quality Enhancement

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Abstract: This paper presents two improved double line voltage synthesis strategies for matrix converters. Both strategies redistribute the on-time intervals of the switches to reduce the output voltage error caused by the limit of minimum safe pulse width during commutation process. The first strategy reconstructs the modulation law according to the relationship between the input and the output voltages. The second strategy takes the current relationship into account, and the on-time intervals are calculated using the instantaneous output currents. Without increasing the commutation times and switching losses, the proposed strategies can decrease the number of pulses whose duty cycles are less than the minimum limit and improve the output voltage waveform. Moreover, the second one can also enhance the input current quality. Numerical simulations and experiments with a 10-kW prototype are carried out. The results are given to verify the feasibility and effectiveness of the proposed strategies.

Keywords: Commutation, Double Line Voltage Synthesis (DLVS) Strategy, Matrix Converter, Power Quality.

I. INTRODUCTION

The matrix converter is a single-stage ac/ac converter. It has attracted motor drive applications due to its high power quality and density, regeneration capability, and compact structure. Recently, the matrix converter has been used in many industrial areas such as wind power generation, elevators, and mechanical manufacture, owing to the further improvement in modulation strategy commutation technology quality of input and output waveforms and operation stability. In the matrix converter, bidirectional switches are adopted to synthesize the expected voltages and control the phase angle of the input current. Related to the bidirectional switches, commutation issues have been raised due to the finite turn on and turn-off time of the switching devices. To provide a path for the conduction of inductive load current and avoid the short-circuit hazard of power supply, a complete commutation process is divided into multiple steps, and a time delay needs to be inserted between the consecutive steps. Similar to the dead-band in PWM inverter, the multistep commutation strategies can give rise to a nonlinearity error between the reference voltage and the actual output. When a motor operated by a matrix converter operates in a low-speed region, the voltage error characterized by voltage distortion and fundamental voltage drop is crucial and results in load current distortion, torque ripple, and additional losses. The issues mentioned above have been investigated in literature. It is shown that the voltage error is primarily due to the following reasons: the switching edge uncertainty, the limit of minimum safe pulse width, and the voltage drop of devices.

At present, various solutions have been proposed which can be classified into three types: simplification of the commutation procedures, pulse width extension by optimizing the switching sequence, and the application of nonlinearity compensation. Simplification of the commutation procedures is a common method. It can weaken the uncertainty in switching edge position and reduce the minimum safe pulse width that appears at the gate driver circuit. In another concept, was proposed based on the knowledge of relative input voltage magnitude. By this method, the traditional four- or two-step commutation techniques can be reduced to three- or single-step ones, respectively. Extending the on-time interval for each switch by optimizing the switching sequence is another solution to overcome the voltage error caused by the minimum pulse width constraint. Suggests an improved double line voltage synthesis strategy (DLVS) which rearranges two zero-voltage switching states in each switching period. This strategy can effectively reduce the nonlinearity error in output voltage, particularly for low speed operation of matrix converter. However, the number of commutations in each switching period and switching losses will increase.

The last method is developed like the average error-voltage compensation for dead time effect of PWM inverter, which needs to build the model of voltage error. In nonlinearity error modelling has been performed considering
the switching edge uncertainty and device voltage drop effect in the d-q and α-β reference frames, respectively. Then, the compensation component is calculated and acts as a voltage feed forward term to cancel the nonlinearity error between the reference voltage and the actual output. The results demonstrate that this compensation technique can enhance the low-speed performance of matrix converter-based motor drives. In this paper, the modulation law of matrix converter is improved to reduce the output voltage error caused by minimum pulse width constraint. Based on the DLVS strategy proposed in an analysis of the influence of pulse width limit and the occurrence of narrow pulse are given in detail. According to the input–output relationship of a matrix converter, two new modulation laws are reconstructed. The analysis results and the waveform improvements due to the proposed methods are verified by numerical simulations and experiments.

![Fig. 1. Simplified circuit of a three-phase to three-phase matrix converter.](image)

**II. DOUBLE LINE VOLTAGE SYNTHESIS OF MATRIX CONVERTER**

A typical three-phase to three-phase matrix converter with nine bidirectional switches allow any input phase to be connected to any output phase as shown in Fig. 1. To avoid input line-to-line short circuits and output open circuits, one and only one switch in every output line is conducting at any time. In practical applications, a filter is usually required to reduce the switching frequency harmonics presented in the input currents. For the DLVS strategy, the input and output phase voltages of a matrix converter are expressed as follows, the subscripts of the currents, imax, mid, and imin are equivalent to ic, ia, and ib, respectively; the subscripts omax, omid, and omin are equivalent to oA, oC, and oB, respectively. The subscripts of the switches, imax, mid, and imin are equivalent to c, a, and b, respectively; the subscripts omax, omid, and omin are equivalent to A, C, and B, respectively. To gain the maximum voltage transfer ratio which is defined by the maximum ratio of output voltage amplitude to input voltage amplitude and which is known as 0.866. vomax or vmin is connected to the base voltage according to the polarity of vbase. Specifically, when vbase is equal to vimax, the switch Somax,imax in Fig. 3 is conducted in the whole switching period, and at the same time, Somin,imin must be left open; when vbase is equal to vmin, the switch Somin,imin is in the switching period, and Somax,imax and Somin,imin are open. Consequently, the input–output relationships of a matrix converter are expressed as follows, depending on vbase. When vbase is equal to vimax

\[
\begin{cases}
v_{\text{base}} = v_{\text{imin}} & v_{\text{base}} \leq v_{\text{imin}} \\
v_{\text{min}} & v_{\text{imin}} < v_{\text{base}} < v_{\text{imax}} \\
v_{\text{base}} = v_{\text{imin}} & v_{\text{base}} \geq v_{\text{imax}}
\end{cases}
\]

The base voltage, vbase, is defined as the input phase voltage with the highest absolute value, i.e.,

\[
v_{\text{base}} = \max(v_{\text{imin}},|v_{\text{imin}}|)
\]

Therefore, in the subscripts of the currents, imax, mid, and imin are equivalent to ic, ia, and ib, respectively; the subscripts omax, omid, and omin are equivalent to oA, oC, and oB, respectively. To avoid input line-to-line short circuits and output open circuits, one and only one switch in every output line is conducting at any time. In practical applications, a filter is usually required to reduce the switching frequency harmonics presented in the input currents. For the DLVS strategy, the input and output phase voltages of a matrix converter are expressed as follows, the subscripts of the currents, imax, mid, and imin are equivalent to ic, ia, and ib, respectively; the subscripts omax, omid, and omin are equivalent to oA, oC, and oB, respectively. The subscripts of the switches, imax, mid, and imin are equivalent to c, a, and b, respectively; the subscripts omax, omid, and omin are equivalent to A, C, and B, respectively. To gain the maximum voltage transfer ratio which is defined by the maximum ratio of output voltage amplitude to input voltage amplitude and which is known as 0.866. vomax or vmin is connected to the base voltage according to the polarity of vbase. Specifically, when vbase is equal to vimax, the switch Somax,imax in Fig. 3 is conducted in the whole switching period, and at the same time, Somin,imin must be left open; when vbase is equal to vmin, the switch Somin,imin is closed in the switching period, and Somax,imax and Somin,imin are open. Consequently, the input–output relationships of a matrix converter are expressed as follows, depending on vbase. When vbase is equal to vimax

![Fig. 2. Segment partition. (a) The twelve 30°-segments within a period of the input voltages. (b) The six 60°-segments within a period of the output voltages.](image)
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Substituting (4) and (6) into (8) and (9) yields

\[
\begin{align*}
\Delta v_{\text{omax}} &= \frac{T_{\text{omin}, \text{imin}} \Delta v_{\text{omax}} + T_{\text{omid}, \text{imid}} \Delta v_{\text{omid}} + T_{\text{omid}, \text{imin}} \Delta v_{\text{omid}}}{T_s}, \quad v_{\text{base}} = v_{\text{imax}} \\
\Delta v_{\text{omin}} &= \frac{T_{\text{omin}, \text{imin}} \Delta v_{\text{omin}} + T_{\text{omid}, \text{imid}} \Delta v_{\text{omid}} + T_{\text{omid}, \text{imin}} \Delta v_{\text{omid}}}{T_s}, \quad v_{\text{base}} = v_{\text{imin}}
\end{align*}
\]

(10)

\[
\begin{align*}
\Delta v_{\text{omax}} &= \frac{T_{\text{omid}, \text{imin}} \Delta v_{\text{omax}} + T_{\text{omid}, \text{imid}} \Delta v_{\text{omid}} + T_{\text{omin}, \text{imin}} \Delta v_{\text{omin}}}{T_s}, \quad v_{\text{base}} = v_{\text{imax}} \\
\Delta v_{\text{omid}} &= \frac{T_{\text{omid}, \text{imin}} \Delta v_{\text{omid}} + T_{\text{omin}, \text{imin}} \Delta v_{\text{omin}}}{T_s}, \quad v_{\text{base}} = v_{\text{imin}}
\end{align*}
\]

(11)

Where

\[
\begin{align*}
\Delta v_{\text{imax}} &= v_{\text{imax}} - v_{\text{imod}} \cdot \quad v_{\text{base}} = v_{\text{imax}} \\
\Delta v_{\text{imid}} &= \begin{cases} v_{\text{imod}} - v_{\text{imin}}, & \text{when } v_{\text{base}} = v_{\text{imin}} \end{cases}
\end{align*}
\]

According to and the relationship between the input and output voltages of a matrix converter can be generalized as

\[
\begin{align*}
\Delta v_{\text{omax}} &= \frac{T_{\text{A} \cdot} \Delta v_{\text{omax}} + T_{\text{B} \cdot} \Delta v_{\text{mid}}}{T_s}, \quad v_{\text{base}} = v_{\text{imax}} \\
\Delta v_{\text{omid}} &= \frac{T_{\text{C} \cdot} \Delta v_{\text{omid}} + T_{\text{D} \cdot} \Delta v_{\text{mid}}}{T_s}, \quad v_{\text{base}} = v_{\text{imin}}
\end{align*}
\]

(12)

where the parameters \(T_{\text{A}}, T_{\text{B}}, T_{\text{C}}, \text{ and } T_{\text{D}}\) denote \(T_{\text{omin}, \text{imin}}, T_{\text{omid}, \text{imin}}, T_{\text{omin}, \text{imid}}, \text{ and } T_{\text{omid}, \text{imid}}\), respectively, when \(v_{\text{base}}\) equals \(v_{\text{imax}}\), while they denote \(T_{\text{omin}, \text{imax}}, T_{\text{omid}, \text{imid}}, T_{\text{omin}, \text{imid}}, \text{ and } T_{\text{omid}, \text{imid}}\), respectively, when \(v_{\text{base}}\) equals \(v_{\text{imin}}\). For the input–output current relationship of matrix converter, the top equations in (5) and (7) are correlated to the other two because the sum of the on-time intervals of the three switches in each output line is \(T_s\) and the sum of three-phase input/output currents is zero. Consequently, (5) and (7) can be generalized as the following form similar to (12)

\[
\begin{align*}
\dot{i}_\text{•} &= \frac{T_{\text{A} \cdot} i_{\text{omax}} + T_{\text{B} \cdot} i_{\text{imid}}}{T_s} \\
\dot{i}_{\text{imid}} &= \frac{T_{\text{C} \cdot} i_{\text{imid}} + T_{\text{D} \cdot} i_{\text{imod}}}{T_s}
\end{align*}
\]

(13)

where the subscript \(•\) denotes min or max; specifically, \(•\) indicates min when \(v_{\text{base}}\) equals \(v_{\text{imax}}\), while \(•\) indicates max when \(v_{\text{base}}\) equals \(v_{\text{imin}}\). Let the on-time intervals \(T_{\text{A}}, T_{\text{B}}, T_{\text{C}}, \text{ and } T_{\text{D}}\) satisfy that

\[
\frac{T_{\text{B}}}{T_{\text{A}}} = \frac{T_{\text{D}}}{T_{\text{C}}} = \alpha
\]

(14)

where \(\alpha\) is defined as the current distribution factor. From (13) and (14), the current distribution factor can be expressed by

\[
\alpha = \begin{cases} \frac{i_{\text{imid}}}{i_{\text{imin}}}, & \text{when } v_{\text{base}} = v_{\text{imax}} \\
\frac{i_{\text{imid}}}{i_{\text{imod}}}, & \text{when } v_{\text{base}} = v_{\text{imin}}
\end{cases}
\]

(15)
Under the unity power factor operating condition, current distribution factor in (15) can be calculated as

\[
\alpha = \begin{cases} 
\frac{i_*_{\text{imid}}}{i_{\text{imin}}}, & \text{if } \frac{v_{\text{imid}}}{v_{\text{imin}}} = \frac{v_{\text{base}}}{v_{\text{imin}}} \\
\frac{i_*_{\text{imin}}}{i_{\text{imin}}}, & \text{if } \frac{v_{\text{imin}}}{v_{\text{imin}}} = \frac{v_{\text{base}}}{v_{\text{imin}}} 
\end{cases}
\]  

(16)

where \(i_*\) imax, \(i_*\) imid, and \(i_*\) imin are the input current references. Substituting the line-to-line output voltage references \(\Delta v_{\text{omax}}\) and \(\Delta v_{\text{omid}}\) into (12) yields

\[
\Delta v_{\text{omax}}^* = \frac{T_A \Delta v_{\text{imax}} + T_B \Delta v_{\text{imid}}}{T_s} 
\]

(17)

\[
\Delta v_{\text{omid}}^* = \frac{T_C \Delta v_{\text{imax}} + T_D \Delta v_{\text{imid}}}{T} 
\]

(18)

According to (14), (17), and (18), TA, TB, TC, and TD can be calculated by

\[
\begin{align*}
T_A &= \frac{\Delta v_{\text{omax}} T_s}{\Delta v_{\text{imax}} + \alpha \Delta v_{\text{imid}} T_s} \\
T_B &= \frac{\Delta v_{\text{imid}} T_s}{\Delta v_{\text{imax}} + \alpha \Delta v_{\text{imid}} T_s} \\
T_C &= \frac{\Delta v_{\text{omid}} T_s}{\Delta v_{\text{imid}} T_s} \\
T_D &= \frac{\Delta v_{\text{omax}} T_s}{\Delta v_{\text{imid}} T_s}
\end{align*}
\]  

(19)

Using double- and single-sided PWM patterns, the synthesis of the output line voltages in a switching period is shown in Fig. 4(a) and (b), where \(T_0\)max and \(T_0\)mid indicate the action intervals of zero voltages, which is equal to \(T_s - TA - TB\) and \(T_s - TC - TD\), respectively.

III. COMMUTATION AND MINIMUM PULSEWIDTH CONSTRAINTS

The bidirectional switches of matrix converter are considered as the arrangement in Fig. 5(a), which consists of two IGBTs with series diode in anti parallel connection. When the output phase, according to the DLVS strategy, has to be commutated from one input phase to another, two basic rules that the input phases must never be short circuited and the output phases must not be left open need to be followed.

Four step commutation strategy based on the output current or input voltage sign measurement is often used to complete commutation safely. Their timing diagrams are shown in Fig. 5(b) and (c), in which the current is supposed to flow from the input side to the output side. In Fig. 5, the time delay between each step is defined as the commutation time, \(t_c\). Since power semiconductor is not an ideal switch, the turn-on time and turn-off time are not strictly identical, which can cause short circuit between input phases of matrix converter if the incoming device are turned on before the outgoing device are turned off. Four-step commutation strategy adds \(t_c\) to the control scheme, then the conducting overlap of devices caused by the unsymmetrical turn-on and turn-off time of the devices can be avoided, as the outgoing device will be definitely turned off during \(t_c\).

To find out a proper \(t_c\) is a challenging task because it should be chosen to satisfy the safety of switching, and meanwhile, to be as small as possible to reduce its effect on output voltage. Referring to “dead time” calculation of ac–dc–ac converters, it can be set to be a 20% increase of the maximum difference between turn-off and turn-on delay of the devices [1]. The choice of \(t_c\) depends greatly on the device’s technology and power range. As far as an ac–dc–ac converter is concerned, the dead time for GTO devices can be beyond 40 \(\mu s\), far larger than that for IGBT device, which is normally 2–7 \(\mu s\). Taking a power semiconductor manufacture, Infineon, as an example, the typical value of dead time for a 600-V IGBT is 325 ns, and a dead time of 1 \(\mu s\) to 1.5 \(\mu s\) is sufficient for most applications.
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Fig. 6. Abnormal timing sequence of the commutation strategies due to the pulses shorter than the minimum commutation time. (a) Four-step commutation strategy based on the output current sign measurement. (b) Four step commutation strategy based on the input voltage sign measurement.

For the matrix converter, the minimum time for a complete commutation sequence is $T_d$, which is the triple of $t_c$, so the minimum on-time intervals of the devices should be greater than or equal to $T_d$. If not, faulty commands will be probably exerted on discrete devices, as shown in Fig. 6, resulting in open circuit or short circuit issues. The pulse whose on-time interval is less than $T_d$ is defined as narrow pulse. As far as the DLVS strategy is concerned, the occurrence of narrow pulses is influenced by the following aspects:

- **Modulation strategy**: As shown in and Fig. 2(a), the current distribution factor $\alpha$ changes periodically between zero and one with six times $t_c$ frequency of input voltage. Inevitably, TB and TD become shorter than $T_d$ periodically regardless of the output voltage reference.

- **Output voltage reference**: According to, the on time intervals $T_A$, $T_B$, $T_C$, and $T_D$ are proportional to $\Delta v_{omax}$ or $\Delta v_{omid}$. When the voltage reference is very small compared with the input voltage, the intervals tend to be less than $T_d$. On the other hand, when the references increase, close to 0.866 times of input voltage, the action intervals of zero voltages, $T_{omid}$ become shorter than $T_d$.

- **PWM pattern**: Single- and double-sided PWM patterns generate different pulse commands for the same bidirectional switch. In Fig. 4(a), by using double-sided PWM pattern, switch $S_{omax,imid}$ and $S_{omid,imid}$ acts twice in each cycle time, $T_s$, and the period for each conduction is $TB/2(TD/2)$.

The total conduction time for $S_{omax,imid}$ and $S_{omid,imid}$ in $T_s$ is $TB$ and $TD$, respectively. By using single-sided PWM pattern, the switch acts only once, and the conduction period is $TB$ ($TD$ for $S_{omid,imid}$). As a result, double-sided PWM pattern cause more narrow pulses than single-sided PWM pattern with respect to same output voltage reference. However, double-sided PWM pattern is still widely used in practical as it reduces harmonics effectively. Consequently, the narrow pulse problem is unavoidable and should be solved for the DLVS strategy. Traditional solutions against narrow pulses either eliminate them or fix them at an acceptable pulse width. Fig. 7(a) and (b) show the pulse elimination method that limits pulses narrower than $T_d$ and the pulse limiting method that limits narrow pulse width to $T_d$, respectively. As shown in Fig. 7, due to the traditional solutions against narrow pulses and the commutation process, an error exists between the actual voltage and reference voltage, which causes output voltage distortion.

**IV. A STRATEGY IMPROVED DLVS STRATEGY FOR OUTPUT QUALITY**

**A. Strategy Improved DLVS Strategy for Output Quality**

Enhancement For the DLVS strategy, the output line-to-line voltages, $\Delta v_{omax}$ and $\Delta v_{omid}$ are synthesized by input line-to-line voltages, $\Delta v_{imax}$, $\Delta v_{imid}$, and the zero voltage in each switching period. When the action interval of the aforementioned input voltages is shorter than $T_d$, the modulation law is redistributed to reduce voltage error and the number of narrow pulses. Using the double-sided PWM pattern, the proposed strategy is described as follows:

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1. The on-time intervals $T_B$ and $T_D$ are the action interval of $\Delta v_{mid}$. When $T_B/2$ is shorter than $T_d$, it is forced to zero, and the same with $T_D/2$. In order to ensure the desired output voltages, the other two action intervals of $\Delta v_{imax}$ and the zero voltage are redistributed according

$$
\begin{align*}
T'_A &= \frac{\Delta v'_{omax}}{\Delta v_{imax}} T_s, \quad T'_{0_{max}} = T_s - T'_A \\
T'_C &= \frac{\Delta v'_{omid}}{\Delta v_{imax}} T_s, \quad T'_{0_{mid}} = T_s - T'_C
\end{align*}
$$

(20)  
(21)

2. The on-time intervals $T_A$ and $T_C$ are the action intervals of $\Delta v_{imax}$. When $T_A$ or $T_C$ is shorter than the commutation time $T_d$, $\Delta v_{omax}$ or $\Delta v_{omid}$ is indeed close to zero. In this case, only the zero voltage is used to generate the output voltage, as

$$
\begin{align*}
T'_A &= 0, \quad T'_B = 0, \quad T'_{0_{max}} = T_s \\
T'_C &= 0, \quad T'_D = 0, \quad T'_{0_{mid}} = T_s
\end{align*}
$$

(22)  
(23)

3. The on-time intervals $T_{0_{max}}$ and $T_{0_{mid}}$ are the action intervals of zero voltage. When the output voltage reference is very large, the zero voltage will hardly act so that it can be neglected. For example, Fig. 11(a) shows the switching commands of the traditional DLVS and strategy A under the condition that $T_D/2$ is shorter than $T_d$. In this case, the conduction time of $S_{omax,imax}$, $S_{omid,imid}$, and $S_{omax,imin}$ remains the same as the calculation results of the traditional DLVS because $T_A$ and $T_B/2$ are greater than $T_d$; while the conduction time of $S_{omid,imax}$, $S_{omid,imid}$, and $S_{omid,imin}$ is derived from (21). For strategy A, the redistributed on-time intervals do not satisfy the input current control requirement shown in (14) and (16), which leads to input current distortions.

MATLAB circuit diagram and input output diagrams as shown in Figs. 8 to 10.

**Matlab circuit diagram:**

![Matlab circuit diagram](image_url)

**Matlab input:**

![Matlab input](image_url)

**Matlab output:**

![Matlab output](image_url)

**Fig. 9. Matlab input.**  
**Fig. 10. Matlab output.**

**B. Strategy**

B: Improved DLVS Strategy for Input and Output Quality Enhancement For the DLVS strategy, the relationship between input and output currents is given in (13), which can also be rearranged as follows:

$$
\begin{align*}
\frac{i_{omid}}{i_*} &= \frac{T_B i_{omid} + T_D i_{imid}}{T_A i_{omax} + T_C i_{omid}}
\end{align*}
$$

(24)

By substituting (16) into (28), the following expression is obtained under the unity power factor operating condition

$$
\begin{align*}
\alpha &= \frac{T_B i_{omid} + T_D i_{imid}}{T_A i_{omax} + T_C i_{omid}}
\end{align*}
$$

(27)
2. Infinite representations: the output currents provide a degree of freedom to define the modulation strategy. Concretely, the representations of on-time intervals that satisfy (17), (18), and (29) are not unique; hence, this degree of freedom can be used to reconstruct the modulation law to reduce the number of narrow pulses and improve the input and output waveforms. The on-time intervals calculated using output currents are defined as T_A, T_B, T_C, and T_D. One of T_A, T_B, T_C, and T_D is set to be zero in turn, the other three from (17), (18), and (29) are solved, and then the four groups of redistributed on-time intervals are obtained which satisfy the output voltage reference and the expected input current at the same time. For example, when T_D is equal to zero, the redistributed on-time intervals are calculated as

\[
\begin{align*}
T_A &= T_A - T_{mid} \\
T_B &= T_B + T_{mid} \\
T_C &= \frac{\alpha + \Delta v_{mid}}{\alpha - \Delta v_{mid}} T_{mid} \\
T_D &= 0.
\end{align*}
\]

Where T_A and T_B are provided by (19)

A variable \( \beta \in [0,1] \) is defined as

\[
\beta = \frac{\min(\mid v_{mid} - v_{imin} \mid , \mid v_{max} - v_{imin} \mid , \mid v_{max} - v_{mid} \mid , \mid v_{mid} - v_{imin} \mid )}{v_{base} = v_{imax}}
\]

As shown in (31), \( \beta \) can be differently expressed depending on the instantaneous relationship among the output currents; therefore, when (31) is substituted (30), (30) can be rewritten into four sets of expressions according to instantaneous output currents, as shown in the last row of Table I. Similarly, the first three rows in Table I also present the redistributed on-time intervals under the constraint conditions that T_A, T_B, and T_C equal zero, respectively. S is discussed in Section III, a small value of \( \alpha \) or/and \( \Delta v_{mid} \), in a switching period, makes different on-time intervals become shorter than Td. Specifically, according to (19), when \( \alpha \) is very close to zero, T_B and T_D simultaneously become shorter than Td; when \( \Delta v_{mid} \) is very close to zero, T_C and T_D are shorter than Td at the same time; when \( \alpha \) and \( \Delta v_{mid} \) are both close to zero, T_B, T_C, and TD are simultaneously shorter than Td; when neither \( \alpha \) nor \( \Delta v_{mid} \) is close to zero, but \( \alpha \Delta v_{mid} \) is very small, only TD is shorter than Td. The proble of narrow pulses caused by the above four cases can be solved to some extent by using various sets of redistributed on-time intervals according to their features. To reveal the features of redistributed on-time intervals in Table I, each set of expressions in the last row, for example, will be analyzed according to the instantaneous outputcurrents.

- The output currents satisfy \( |io| \geq |iomid| \) and \( |io| \cdot iomid \geq 0 \): according to the expressions given in column 1, it can be seen that, T_A ad T_C, the new action intervals, re both increased to a certain extent, which has the advantage of reducing the number of narrow pulses caused by the above four cases.
- The output currents satisfy \( io \cdot iomid < 0 \): as can be seen in columns 2 and 4, the value of T_C is increased due to the reduction of the denominator, while T_B is decreased.
TABLE I: Redistributed On-Time Intervals under The Condition That $T_A$, $T_B$, $T_C$, And $T_D$ Dequal Zero, Respectively

| Conditions | $i_{oA} \cdot t_{oA} \geq |i_{oM}|$ | $i_{oA} \cdot t_{oA} < |i_{oM}|$ | $i_{oA} \cdot t_{oA} \geq |i_{oM}|$ | $i_{oA} \cdot t_{oA} < |i_{oM}|$ |
|------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| $T_A = 0$  | $T_A = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_A$ | $T_A = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_A$ | $T_A = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_A$ | $T_A = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_A$ |
| $T_B = 0$  | $T_B = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_B$ | $T_B = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_B$ | $T_B = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_B$ | $T_B = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_B$ |
| $T_C = 0$  | $T_C = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_C$ | $T_C = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_C$ | $T_C = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_C$ | $T_C = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_C$ |
| $T_D = 0$  | $T_D = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_D$ | $T_D = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_D$ | $T_D = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_D$ | $T_D = \frac{N_{max}}{N_{max} + \alpha N_{max}} T_D$ |

VI. SIMULATION RESULTS

To verify the feasibility and performance of the two proposed strategies, a Matlab/Simulink simulation for the matrix converter with R-L load was performed. In the simulation, the current commutation is accomplished with the strategy based on the output current sign measurement.

TABLE II: Simulation Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMS of input line voltage $V_i$</td>
<td>100 V</td>
</tr>
<tr>
<td>Frequency of input voltage $f_i$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Filter choke $L_f$</td>
<td>1.5 mH</td>
</tr>
<tr>
<td>Filter capacitor $C_f$</td>
<td>10 μF</td>
</tr>
<tr>
<td>Load resistor $R_L$</td>
<td>10 Ω</td>
</tr>
<tr>
<td>Load inductor $L_L$</td>
<td>40 mH</td>
</tr>
<tr>
<td>Frequency of output voltage reference $f_o$</td>
<td>25 Hz</td>
</tr>
<tr>
<td>Switching period $T_s$</td>
<td>200 μs</td>
</tr>
</tbody>
</table>

The switching characteristics of the semiconductors are also taken into account. The parameters used in simulation are listed in Table III. In this paper, the occurrence of the pulses whose width is less than 3 μs is studied in function of the value of voltage transfer ratio. In Fig. 12, the narrow pulse distributions of both proposed strategies are given compared with those of the traditional DLVS strategies using different PWM patterns at various voltage transfer ratios. As shown in Fig. 12, narrow pulses exist in the traditional DLVS strategy within the whole range of voltage transfer ratio. Moreover, the number of narrow pulses is large, particularly at low-voltage transfer ratio.

![Fig. 12. Simulated input and output currents of the matrix converter for different strategies with the voltage transfer ratio being 0.2, $T_d$ being 6 μs.](image-url)
Improved Double Line Voltages Synthesis Strategies of Matrix Converter for Input/Output Quality Enhancement

Fig. 1. Matrix converter prototype.

Fig. 13. Matrix converter prototype.

Fig. 14. Experimental results of the matrix converter for different strategies with voltage transfer ratio being 0.2, Td being 2.4 μs, input voltage (34.5 V/div), input current (0.98 A/div), output current (0.625 A/div). (a) DLVS strategy utilizing the pulse elimination method. (b) DLVS strategy utilizing the pulse limiting method.

For example, when the voltage transfer ratio is 0.2, pulses short than 3 μs occupy about 14.3% of the distribution using double sided PWM patterns, while the percentage is reduced to 0 and 4.7% by using strategies A and B, respectively; hence, it can be concluded that the two proposed strategies can effectively reduce the number of narrow pulses. In particular, strategy A can eliminate all narrow pulses within the whole range of voltage transfer ratio. Here, it should be pointed out that the narrow pulses shorter than Td exist in strategy B. In such cases, additional solutions against the narrow pulses, such as the pulse elimination method, should be utilized.

Fig. 15. Experimental results of the matrix converter for different strategies with voltage transfer ratio being 0.8, Td being 2.4 μs, input voltage (34.5 V/div), input current (1.96 A/div), output current (2.5 A/div). (a) DLVS strategy utilizing the pulse elimination method. (b) DLVS strategy utilizing the pulse limiting method. (c) Strategy A. (d) Strategy B.

Fig. 16. Experimental results of the matrix converter for different strategies with voltage transfer ratio being 0.2, Td being 6 μs, input voltage (34.5 V/div), input current (0.98 A/div), output current (0.625 A/div). (a) DLVS strategy utilizing the pulse elimination method. (b) DLVS strategy utilizing the pulse limiting method. (c) Strategy A. (d) Strategy B.

To evaluate the output power quality, the output current total harmonic distortion (THD) of the two proposed strategies is given in Fig. 13, compared with those of DLVS utilizing the pulse elimination method and the pulse limiting method at various voltage transfer ratios. In the simulation, the minimum commutation time Td is set as 2.4 μs. From Fig. 13, the output power quality is improved by using the proposed strategies particularly at low-voltage transfer ratios. Furthermore the output power quality of strategy A is better than that of strategy B since narrow pulses are completely
eliminated by strategy A. In Fig. 14, a similar comparison in terms of input current THD is presented under the same simulation conditions. The input current THD of strategy B is always the lowest compared with that of other strategies, which verifies that strategy B can improve input current quality. In Fig. 15, the simulated input and output currents of matrix converter utilizing different strategies are given with the voltage transfer ratio being 0.2. The influence of minimum pulsewidth constraint $T_d$ on the power quality is analyzed as follows. Fig. 16 provides the input and output currents of different strategies with $T_d$ being 6 $μ$s. In this case, about 36% of the pulses are shorter than the constraint by using the traditional DLVS strategy with double sided PWM patterns. Compared with the results in Fig. 15, the currents of the pulse elimination method and the pulse limiting method are significantly distorted. For strategy A, pulsewidth constrain barely deteriorates output quality, but input current is slightly distorted because the rearranged on-time intervals do not meet the input current control requirement. For strategy B the harmonic content of the input and output currents becomes a little higher as $T_d$ is increased.

VII. CONCLUSION

Two improved DLVS strategies have been presented to reduce the output voltage errors of matrix converter caused by the minimum pulsewidth constraint. The first one (strategy A) redistributes the on-time intervals of bidirectional switches according to the demand for the output voltages. This strategy can be easily implemented. The second method (strategy B) redistribute the on-time intervals according to the output voltage and input current control requirement. This strategy is more complicated for implementation and requires the measurement of instantaneous output currents. For both strategies, the number of narrow pulses can be effectively reduced without increasing commutation times and switching losses, compared with the traditional DLVS strategy. Numerical simulations and experiments with a 10 kW prototype are carried out. The results confirm that both strategies are feasible and effective. The first method yields relatively better output voltages and, in consequence, sinusoidal currents even with a large $T_d$. The second method is an improved version of the first one. It obtains better input current which is more sinusoidal with lower harmonics. However, the performance of this method depends on selection of minimum pulse width constraint.

VIII. REFERENCES


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Improved Double Line Voltages Synthesis Strategies of Matrix Converter for Input/Output Quality Enhancement

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