Space Vector PWM Based Voltage Balancing Ability with Natural Capacitor in A Four Level Hybrid Clamped Converter

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Abstract: In this paper we present a new topology to generate four level PWM AC output from less number of components. In conventional inverters for four level output more number of power electronic devices are used, which may lead to switching losses and also increase in harmonic distortion. To operate the converter phase shift space vector pulse width modulation technique is used for generation of pulses fed to power electronic devices. Analysis of a single phase induction machine is carried out with four level space vector PWM input and THD is calculated.

Keywords: Medium-Voltage (MV), ANPC, PWM.

I. INTRODUCTION

Energy saving has never been more important than it is today. In industrialized countries, about 70% of all of the generated electric energy is used by electrical motors. In addition, more than 60% of all the electric energy converted into mechanical energy is consumed by pump and fan drives with induction motors. This fact points out the importance of energy savings in these types of drives. High power pumps and fans need medium-voltage (MV) Drives. At this rating, MV machine designs offer significant cost savings and improvements in the thermal performance of their power components. The switching devices are connected in series to raise the blocking capacity in conventional two-level MV inverters. The simultaneous switching of series connected fast devices generates voltage with a high dv/dt at the output terminal of the inverter. The combination of a short rise time of the inverter output voltage and a long cable are potentially hazardous for the motor insulation and the cable itself. The phenomenon, which is worsened with a shorter rise time, appears on motors as a leakage current. In motor drive applications, this may lead to electromagnetic interference noise that causes a nuisance trip of the inverter drive, problems with the protection scheme of the supply transformer and interference with other electronic equipment in the vicinity.

In order to avoid the series connection of two switches in the five-level ANPC converter, this paper presents a novel four-level hybrid-clamped converter for medium-voltage motor drives, as shown in Fig. 1. Compared to the five-level ANPC converter, this four-level hybrid-clamped converter contains only eight switches and the nominal voltages across the upper and lower dc-link capacitors are the same as the flying capacitor, hence each switch withstands the same voltage stress. In the other hand, in order to increase the voltage levels, an extra capacitor is inserted into the dc-link so that each phase can output four voltage levels.

This four-level hybrid-clamped topology can also be regarded as a modification of four-level flying-capacitor topology. The high-voltage flying capacitor near the dc-link is replaced by two clamping switches, hence the total size and weight can be reduced. Compared to four-level diode-clamped converter, the proposed topology also has many advantages. Four-level diode-clamped converter need six clamping diodes per phase and each voltage level only corresponds to one switching state, which makes it difficult to balance the dc-link capacitor voltages [19],[20]. The proposed four-level hybrid-clamped converter uses only two switches and a flying capacitor for clamping and has plenty of redundant switching states, which makes it possible to balance the dc-link and flying capacitor voltages. This paper is a major revision of conference paper [21], including a detailed introduction of modulation method and an in-depth analysis of natural capacitor voltage balancing ability. More experimental results are also presented in this paper. This paper is organized as follows. In Section II, the operating

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principle of this converter is introduced. The modulation method and natural balancing of capacitor voltages using PSPWM are discussed in Section III. Some experimental results under different frequency and modulation index are presented in Section IV. Section V presents a comparison of several multilevel topologies for medium-voltage motor drives.

II. CONTROL AND OPERATING MODES OF PROPOSED TOPOLOGY

Considering a single phase and defining the switching function of switch $S_x$ is $S_{fx}$, where $x$ represents 1–8, the instantaneous output voltage level $V_o$ can be written as the sum of voltages across switches $S_1$, $S_2$, and $S_3$:

$$V_o = (S_1 + S_2 + S_3)E.$$  \hfill (1)

The above equation indicates that the output voltage level is determined by the sum of the switching functions $S_1$, $S_2$, and $S_3$. Moreover, switches $S_1$, $S_2$, and $S_3$ are independent of each other so that classical PS-PWM can be used to control this converter. The PS-PWM was widely used in flying-capacitor multilevel converters and cascaded H-bridge converters for its natural capacitor voltage balancing and power equalization ability [22]–[26]. What is more, it is a modular modulation scheme and easy to implement. Each switch pair can be controlled as a two-level cell independently and the transition of different switching states does not need to be considered. For an n-level multilevel converter, a reference modulation signal is compared to $n-1$ triangular carrier signals that are phase shifted by $2\pi/(n-1)$. The resulting signals are used to control the corresponding switches as shown in Fig. 2.

For the flying capacitor $C_f$, the load current flows out of it when $S_3$ and $S_5$ are switched ON and into it when $S_2$ and $S_4$ are switched ON. So the instantaneous flying capacitor current $i_{cf}$ can be written as

$$i_{cf} = (S_5 - S_2) \cdot i_o.$$  \hfill (2)

For the dc-link capacitors, the load current flows out of neutral point $N_1$ when $S_7$ and $S_2$ are switched ON and OUT of $N_2$ when $S_8$ and $S_5$ are switched ON. So the instantaneous neutral-point currents ($i_{N1}$, $i_{N2}$) can be written as

$$i_{N1} = S_{81} (1 - S_{82}) \cdot i_o$$  \hfill (3)

$$i_{N2} = S_{71} (1 - S_{72}) \cdot i_o$$  \hfill (4)

Defining the duty ratio of $S_1$, $S_2$, and $S_3$ are $d_1$, $d_2$, and $d_3$, respectively, based on (2), the average output phase voltage in a carrier period can be written as

$$u_o = (d_1 + d_2 + d_3)E.$$  \hfill (5)

The neutral-point currents are the primary variables which determine the voltage variations of dc-link capacitors. Once the neutral-point currents are known, the NP potential variations can be obtained. In order to verify the natural voltage balancing ability of the dc-link capacitors, the average neutral-point currents in a fundamental period should be considered. The interval division of reference voltage $u_{ref}$ is shown in Fig. 3. When $0 \leq m \leq 1/3$, then $1/3 \leq u_{ref} \leq 2/3$, the average neutral-point currents in a fundamental period $T$ can be calculated.

For the flying capacitor $C_f$, the load current flows out of it when $S_3$ and $S_5$ are switched ON and into it when $S_2$ and $S_4$ are switched ON. So the instantaneous flying capacitor current $i_{cf}$ can be written as $i_{cf} = (S_5 - S_2) \cdot i_o$.

For the dc-link capacitors, the load current flows out of neutral point $N_1$ when $S_7$ and $S_2$ are switched ON and OUT of $N_2$ when $S_8$ and $S_5$ are switched ON. So the instantaneous neutral-point currents ($i_{N1}$, $i_{N2}$) can be written as $i_{N1} = S_{81} (1 - S_{82}) \cdot i_o$ and $i_{N2} = S_{71} (1 - S_{72}) \cdot i_o$.

Fig. 2. PSPWM pulse generation waveforms.

Fig. 3. SVPWM modes of PSPWM.
III. SPACE VECTOR PWM TECHNIQUE

Space vector PWM technique is an advancement of sinusoidal PWM as the pulses produced by digital switching of the fundamental waveform. Considering six switch operation we divide the VSI into two parts as upper part and lower part. The upper part contain the switches S1 S3 & S5 leaving the lower part of the VSI with S2 S4 & S6. The state of the switches are either to be ON or OFF i.e., two states. The number of possible switching states are give as $2^3 = 8$. The 8 switching states are given below:

<table>
<thead>
<tr>
<th>SWITCH</th>
<th>S1</th>
<th>S3</th>
<th>S5</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ST MODE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2ND MODE</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3RD MODE</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4TH MODE</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5TH MODE</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6TH MODE</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>7TH MODE</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>8TH MODE</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

In the above mentioned 8 switching modes the first and the last are completely OFF and ON which is not applicable. We only consider the six states from 1st to 6th eliminating 0 and 7th mode. The last three switching states are the complement of first three switching states, which concludes that we have to only generate the three switching states i.e., 1st, 2nd, and 3rd. The other switching states i.e., 4th, 5th, and 6th are generated by applying a NOT gate to the previous modes. A simple hexagonal representation of switching pattern is shown below Fig.4 which can be called as Space vector Trajectory.

![Fig. 4. Space vector trajectory.](image)

The signal generation of space vector is compared to the triangular waveform to generate three PWM pulses to which NOT gates are given to get the other three pulses. The control signal of space vector PWM is given below Fig.5.

![Fig. 5. Control signals of Space vector PWM.](image)

IV. SIMULATION RESULTS AND OUTPUTS

Simulation results of this paper is shown in bellow Figs.6 to 11.

![Fig. 6. Four level converter with single phase induction motor.](image)

![Fig. 7. Four level PWM output of the topology.](image)

![Fig. 8. Space vector PSPWM pulse generation waveforms.](image)
V. CONCLUSION

With the above analysis and graphical representation the output of the four level topology is shown with THD FFT analysis, with a value of 5.29% harmonic distortion in the main winding current which is very less compared to conventional converters. The Space vector PSPWM technique is utilized to get the maximum amplitude of the output with lesser THD values and precise operation of the switches. The reduction in loss of power, increases the efficiency of the proposed topology.

VI. REFERENCES